Abstract #1883, 224th ECS Meeting, © 2013 The Electrochemical Society

X-ray Characterization of PEALD versus PVD Tantalum Nitride Barrier Deposition and the Impact on Via Contact Resistance

X. Zhang[1], O. van der Straten[2], T. Bolom[1], M. He[1], J. Maniscalco[3], D. Edelstein[2]

[1] *GLOBALFOUNDRIES, 257 Fuller Rd, Albany, NY 12203*

[2] *IBM Research, 257 Fuller Rd, Albany, NY 12203*

[3] *IBM Systems & Technology Group, 257 Fuller Rd, Albany, NY 12203*

As the critical dimension (CD) of features is scaled below 30 nm, significant BEOL integration challenges appear, as well as many difficulties in interconnect metallization, which requires highly controlled metal barrier and seed deposition processes [1]. For the barrier process, an extension of the current physical vapor deposition (PVD) TaN/Ta barrier continues to be preferable. However, an alternative conformal process such as atomic layer deposition (ALD) has seen increased focus in the last few years. A recent comprehensive study has shown the benefit of thermal ALD TaN for via resistance reduction with a relatively thick PVD Ta to enhance the reliability [2].

In a previous study, we have reported on lowering the resistivity of ALD TaN with different direct plasma approaches compared to (remote) PEALD and thermal ALD TaN [3]. In this study, plasma enhanced ALD TaN films were deposited using a mixed remote hydrogen (H_2) and ammonia (NH_3) plasma to reduce pentakis(dimethylamino)tantalum (PDMAT) at 275°C. One PEALD TaN cycle consisted of a PDMAT exposure followed by a H_2 and NH_3 plasma exposure at 600W. Both PEALD TaN and PVD TaN films were deposited on a 300mm clustered metal deposition platform.

Patterned M1/V1/M2 wafers with features at a CD of 32nm were used to compare both PVD and PEALD TaN barriers at M2 level. Via resistance from different wafers were measured at the last BEOL metal level. As shown in figure 1, 10Å PEALD TaN reduced via resistance by 50% compared to the PVD TaN baseline. Originally, a simplified model of reduced via contact resistance by the deposition of a thinner barrier layer at the contact area had been suggested. However, soon it became evident that a more complex mechanism was necessary to be taken into account. Effects such as differences in film nucleation on various surfaces, modulation of barrier interface composition and morphology of the barrier should be considered.

From a film property characterization point of view, the density and resistivity of PEALD TaN film were about 11.6 g/cm^3 and ~2000 μΩ-cm respectively, while Ta-rich PVD TaN had a higher density of about 15.0 g/cm^3 and a resistivity around 250 μΩ-cm. Hence, based on via resistance values observed, the intrinsic electrical resistivity did not play an important role in the total via resistance.

Subsequently the nucleation of ALD TaN was studied using X-ray fluorescence (XRF) to assess the ALD TaN thickness on copper or other potential metal cap materials expected to be present below a via. In order to mimic the nucleation difference between via bottom and sidewall, PEALD TaN was deposited on both metal substrates such as Cu, CuO (Cu without surface clean), Co (as potential metal cap material) and dielectric substrates with dielectric constant from 2.4-2.7. The results in figure 2 showed that metal substrates yielded 30% higher Ta counts compared to dielectric substrates. This may demonstrate that PEALD TaN is actually thicker at the via bottom than on sidewalls which would oppose the hypothesis that the actual thickness of PEALD TaN at a via bottom is negligible.

Therefore, it appears that the interface of Cu and TaN may be of more importance. X-ray reflectivity (XRR) was used to study the potential root cause of the interfacial difference. In figure 3, the spectrum of 20nm PVD TaN was well fitted by a three-layer model, including top surface oxidized layer, bulk film layer and interfacial layer between TaN and silicon oxide substrate. The interfacial layer indicates the presence of a damaged interface introduced by ionized PVD TaN deposition, while the XRR data for PEALD TaN did not show an interfacial layer. In summary, improvements in via resistance when moving from PVD to ALD TaN are likely not due to bulk resistivity or layer thicknesses, but appear to relate to the interface between the TaN and the underlying layer, and the presence (PVD) or absence (ALD) of damage.

This work was performed by the Research Alliance Teams at various IBM Research and Development Facilities.

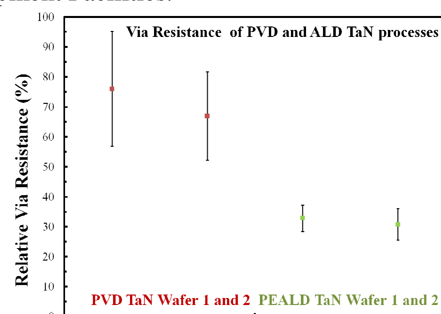

Fig. 1: Via resistance with PVD vs. PEALD TaN barrier.

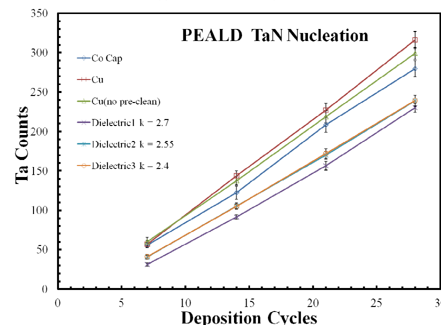

Fig. 2: XRF counts of Ta in PEALD TaN deposited on different substrates (Co, Cu, CuO, dielectrics with k = 2.7, 2.55 and 2.4) vs. deposition cycles.

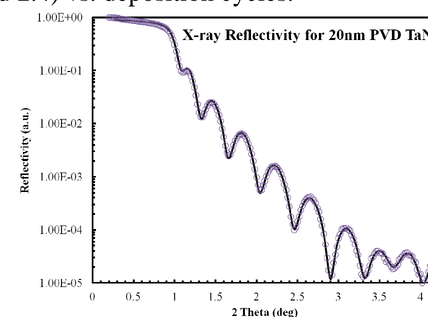

Fig. 3: X-ray reflectivity data of 20nm PVD TaN. Solid line is a fitting of the raw spectrum.

REFERENCES

1. B. Taylor, X. Lin, X. Zhang, M. He, and V. Ryan, Proceedings of the IEEE International Interconnect Technology Conference (IITC) 2012, pp. 1-1 (2012).
2. K. Motoyama, and K. Fujii, ECS J. Solid State Sci. Technol. 2012, 1, pp. 303-309 (2012).
3. O. Van der Straten, X. Zhang, C. Penny, J. Maniscalco, S. Chiang, J. Ren, and P. Ma, ECS Trans. 50, pp. 159-164 (2012)