Abstract #1876, 224th ECS Meeting, © 2013 The Electrochemical Society

Advanced dielectrics targeting 2X DRAM MIM capacitors

Mihaela Popovici, Johan Swerts, Marc Aoulaiche, Augusto Redolfi, Ben Kaczer, Min-Soo Kim, Sergiu Clima, Malgorzata Jurczak, and Sven Van Elshocht
imec
Kapeldreef 75 – B-3001 Leuven – Belgium

Scaling down of dynamic random access memory (DRAM) towards 2X node will require a reduction of both equivalent oxide thickness (EOT) to ≤ 0.45 nm while maintaining a leakage current density (J_g) of ~ 10^{-7}A/cm^2 at ± 1V of the metal-insulator-metal capacitors (MIMCAP). Moreover, the ITRS roadmap recommends a reduction of the physical thickness of the insulator to 7 nm or less. In this respect, the dielectric employed requires a dielectric constant k of at least 60. However, an increase of dielectric constant is commonly associated with a low bandgap, which results in an increase of the leakage current through the dielectric. In spite of the high dielectric constants of at least 80, the low bandgap of~ 3.0-3.2 eV of strontium titanates and rutile TiO_2 makes it difficult to reduce the physical thickness without compromising the leakage current density to fulfill the above mentioned specifications. Another important aspect is the choice of the metal electrode where the work function, thermal stability, absence of interfacial "dead layer" are key factors in improving the performance of the MIMCAPs. Finally, both the dielectric and the metal should be deposited by highly conformal techniques such as Atomic Layer Deposition (ALD).

We have previously shown how the dielectric constant, the bandgap, and the EOT-J_g can be tuned using strontium titanate with variable Sr content in a relatively large range of Sr/(Sr+Ti) ratio between 45-67% Sr using different Sr:Ti pulse ratios [1]. The leakage current exponentially increases with the decrease of Sr content. Nevertheless, we could demonstrate a slower increase of leakage current using a TiO_2/Sr-rich STO stack deposited on a RuO_x/Ru bottom electrode [2]. The STO film with ~54% Sr content is obtained via intermixing of TiO_2 and Sr-rich STO (62% Sr) layers after crystallization anneal, an essential factor to control the grain morphology and the interface metal/dielectric. Besides the dielectric, also the choice of electrode is important as it has been shown that Ru and RuO_2 [3] yield much better results compared to e.g. TiN.

The last ones appear as the most promising candidates. In order to improve EOT-J_g characteristics, other parameters, such as dopants for STO and rutile TiO_2 dielectrics were studied as well.

We could demonstrate an EOT of 0.42 nm and J_g~10^{-6} A/cm^2 when STO is deposited on Ru on a 300 mm wafer with a within wafer non-uniformity, $1\sigma < 5\%$. On the other hand, electron injection from the TiN top electrode show a significantly higher leakage likely due to the oxygen scavenging effect exerted by the TiN on STO.

Another dielectric employed, namely rutile TiO_2, brings the advantage of a lower thermal budget as the crystalline phase is formed directly as grown by atomic layer deposition on Ru. Both dielectrics were deposited at 250 °C in $Ti(OCH_3)_4$ - O_3 (rutile TiO_2) and $Sr(^tBu_3Cp)_2$-$Ti(OCH_3)_4$ - H_2O (STO) reaction systems, respectively [4, 5]. The STO films crystallize in the cubic perovskite structure (k~ 145) and rutile TiO_2 crystallizes in the tetragonal rutile phase (110) textured (k~ 90). Lower k value as compared to literature [6] is attributed to a different texture. Comparing the performance of rutile TiO_2 and STO MIMCAP TiN/Ru (bottom electrode, BE)/dielectric(TiO_2 or STO)/TiN(top electrode, TE) at similar physical thickness (~ 9nm) as deposited (see figure 1), STO show better properties in respect of both EOT and J_g.

Based on our results, STO ALD is highly promising for the industrial implementation of higher-k dielectrics in DRAM MIMCAP with a design rule of 20 nm.

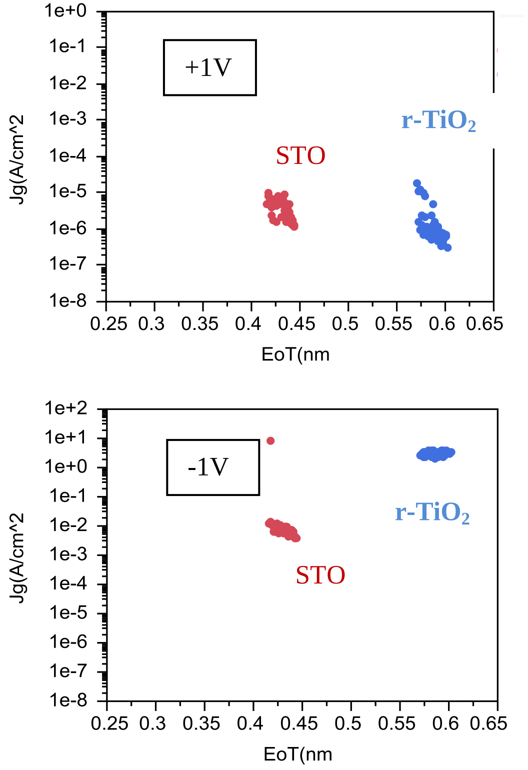

Fig.1. EOT-Jg dependence for the injection from BE (+1V) and TE (-1V), respectively on 59 dies (300 mm diameter wafers).

[1]. N.Menou, M.Popovici, S.Clima, K.Opsomer, W. Polspoel, B. Kaczer, G. Rampelberg, K. Tomida, M. A. Pawlak, C. Detavernier, D. Pierreux, J. Swerts, J. W. Maes, D. Manger, M.Badylevich, V. V. Afanas'ev, T. Conard, P. Favia, H. Bender, B. Brijs, S. Van Elshocht, G. Pourtois, D. J. Wouters, S.Biesemans, and J. A. Kittl, J. Appl. Phys. 106, 094101 (2009).

[2]. M. A. Pawlak, M. Popovici, J. Swerts, K. Tomida, M.-S. Kim, B. Kaczer, K. Opsomer, M. Schaekers, P. Favia, H. Bender, C. Vrancken, B. Govoreanu, C. Demeurisse, W.-C. Wang, V. V. Afanas'ev, I. Debusschere, L. Altimime, and J. A. Kittl, Tech. Dig. - Int. Electron Devices Meet., 277 (2010).

[3]. W. Lee, J.H. Han, W. Jeon, Y. W. Yoo, S. W. Lee, S. K. Kim, C.-H. Ko, C. Lansalot-Matras, C. S. Hwang, Chem. Mater., 25, 953 (2013).

[4]. M. Popovici, S. Van Elshocht, N. Menou, J. Swerts, D.Pierreux, A. Delabie, B. Brijs, T. Conard, K. Opsomer, J. W. Maes, D. J. Wouters, and J. A. Kittl, J. Electrochem. Soc. 157, G1 (2010).

[5]. M. Popovici, M. S. Kim, K. Tomida, J. Swerts, H. Tielens, A. Moussa, O. Richard, H. Bender, A. Franquet, T. Conard, L. Altimime, S. Van Elshocht and J. A. Kittl. Microelectron. Eng., 88, 1517 (2011).

6. J. Aarik, B. Hudec, K. Husekova, R. Rammula, A. Kasikov, T. Arroval, T. Uustare, K. Frohlich, Semiconductor Science And Technology, 27, 074007 (2012).