GaN Power Transistors with Integrated Thermal Management

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GaN power transistors offer great promise for applications in compact, high efficiency power systems simply based upon the properties of III-N materials. These properties result in a power figure-of-merit that is almost 700X greater than silicon and 160X that of 4H silicon carbide. Despite this promise there remain several challenges to reliable GaN power switches including reducing the thermal limit to ultimate performance, reducing gate and forward blocking leakage and reducing the on-resistance of the device. This paper will present recent efforts to address GaN power switch limitations through the development of an enhancement-mode (e-mode) lateral HEMT with integrated nanocrystalline diamond coatings for thermal management – a schematic of which is shown in Figure 1.

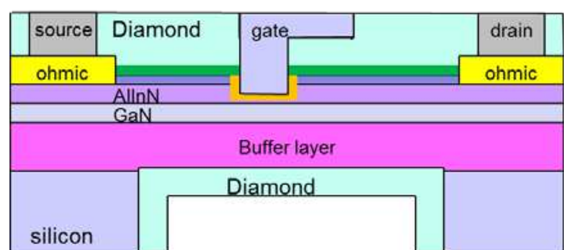

Fig. 1. Schematic cross-section of GaN power transistor with integrated nanocrystalline diamond coatings.

Key elements of this device include the gate dielectric and surface passivation, barrier design for e-mode operation and integration of NCD on both the front-side and back-side of the chip. Each of these elements must be developed and integrated while maintaining acceptable device performance.

E-mode operation requires that the gate be biased both positively and negatively with minimal leakage. To this end, high-k gate dielectrics of Al_2O_3 and HfO_2 have been developed using atomic layer deposition on both GaN and AlGaN surfaces. The goal of these efforts is to develop a dielectric/semiconductor stack that exhibits the lowest gate leakage levels possible with minimal hysteresis and interface charge. For both semiconductor surfaces, surface pre-treatment is essential with each requiring a specific ex situ treatment (piranha etch for GaN, HF for AlGaN). In addition, post-deposition anneals (600°C in N_2 for 60 sec) are found to improve the performance of the dielectric/semiconductor interface. Using these conditions hysteresis as small as 0.03V, interface trap densities below 10^{11} cm^{-2} and leakage current densities of $<10^{-7}$ A/cm^2 have been achieved.

In order to maintain a low on-resistance in an e-mode device it is essential to keep the conductivity of the access regions as low as possible. Further, because GaN power switches offer the advantage of a high switching frequency, it is important to minimize any dispersion in the device's operation due to surface states. Both these issues must be addressed through passivation approaches in the gate-drain and gate-source surface regions of the device. In the case of our diamond integrated HEMT, it is also important that the passivation solution be compatible with the diamond growth process. We have evaluated a number of passivation approaches including silicon oxides and silicon nitrides (PECVD and MOCVD), but have found interesting recent results using AlN passivation layers deposited by atomic layer epitaxy (ALE). Using these layers we demonstrate lower sheet resistance (10%), lower off-state leakage (100X) and reduced dynamic on-resistance degradation (50%) compared to conventional SiN_x passivations.

In order to simultaneously ensure normally-off and high on-state current density operation, the design of the HEMT barrier becomes complex involving AlN interlayers, lattice-matched AlInN ternaries and ultrathin GaN etch stop layers. We will present our barrier design and results on the growth of these critical layers by ALE where ultra-thin film growth is accomplished layer-by-layer.

Aiming for high power operation is only worthwhile if the thermal limitations of even a high efficiency GaN power switch are mitigated. The primary objective is to effectively remove the heat from its source (drain edge of the gate) to heat sinks. We have employed top-side NCD (in our gate-after-diamond) approach to achieve 20% (25-50°C) reductions in device operating temperature while actually enhancing the devices operation (both DC and RF), Figure 2. This is achieved through improved heat spreading from the source to contact pads with simultaneous improvement in sheet resistance and surface passivation. Finally, we will highlight our most recent efforts to further improve upon thermal management through the use of back-side NCD-filled vias for heat extraction to a heat sink.

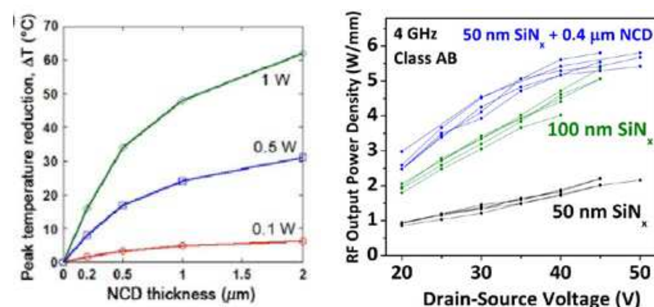

Figure 2. (left) Peak temperature reduction in GaN power switch with NCD top-side coating for various operating powers. (right) RF output performance for GaN HEMT with NCD top-side coating compared to conventional SiNx passivation.

These results offer great promise for the realization of GaN power switches that can perform at near-theoretical levels and, therefore, the promise of GaN power switches for high-power, high-efficiency, compact power conversion systems.

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