Basal Plane Dislocation Mitigation using High Temperature Annealing in 4H-SiC Epitaxy

N. A. Mahadik[a], A. Nath[b], E. A. Imhoff[a], R. E. Stahlbush[a], and R. Nipoti[c]
[a]Naval Research Laboratory, Washington, DC, USA
[b]George Mason University, Fairfax, Va, USA
[c]CNR-IMM Bologna, Bologna, Italy

Basal plane dislocations (BPD) in 4H-silicon carbide (SiC) epilayers cause formation of stacking faults (SF) during device operation, which leads to forward voltage degradation in minority carrier devices [1, 2]. More than 90% of the BPDs in the substrate are converted to benign threading edge dislocations (TED) at the beginning of the epigrowth [3]. For epitaxial growth on 4 degree offcut substrates, BPD to TED conversion is highly enhanced with almost all of them converting in the first 20 μm[4]. However, BPDs in the many areas of the epilayers are often > 100 cm^{-2}, which adversely affects the device yield and reliability. We report on post growth high temperature annealing to remove or shorten BPDs in the epilayers that propagated from the substrate.

We used 4 and 8 degree offcut, 15 μm, n-type 6E15 4H-SiC epilayers. The as-grown samples were imaged using ultraviolet photoluminescence (UVPL) imaging, which shows the BPDs in the epitaxial layers. Carriers were excited with the 334 nm line from an Ar-ion laser, and images were collected in the emission range of 600-1000 nm. Some of the samples were phosphorus implanted for a uniform doping concentration of ~$2x10^{20}$ /cm^3 up to 0.2μm from the sample surface. The samples were graphite capped and annealed at 1600 °C-1950 °C for 30-120s using microwave annealing. Post-annealed samples were also imaged to observe the BPDs in the epilayers.

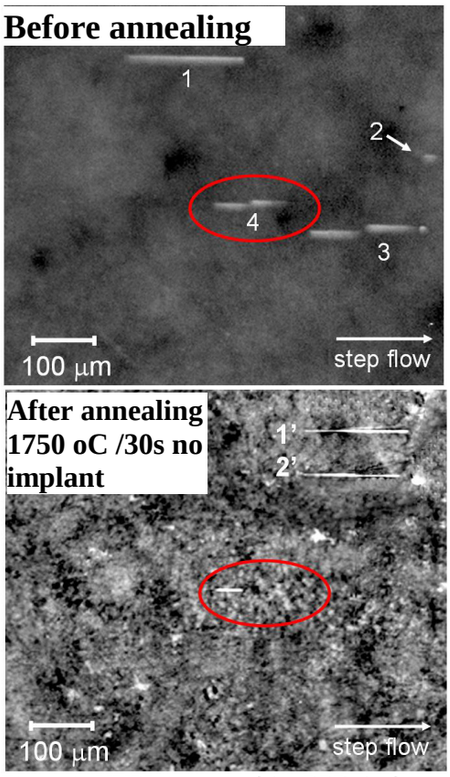

Figure 1: UVPL images of the BPDs before and after MW annealing. Three BPDs (1-3) that had propagated into the epilayers from the substrate disappear. BPD #4 that had propagated 9.3 μm into the epilayer is shortened to 4 μm. Two new BPDs (1', 2') are seen after annealing.

The UVPL images of the as grown samples showed an average BPD density ~1000 /cm^2 in the 4 degree offcut epilayers. Upon high temperature annealing the UVPL images of the samples had a complex structure, where most of the BPDs that were previously present disappeared or were greatly shortened. It is proposed that upon annealing the BPDs that had not yet converted to a TED during epigrowth forms a TED near the surface. Then during the annealing, the TEDs at the end of all the BPDs, that were previously in the epilayer, move towards the substrate-epilayer interface along the basal plane, which shortens the BPD. The UVPL images of the annealed samples show a dot where the original BPD had propagated from the substrate, which represents a TED. This effect of BPD removal was observed in all the annealed samples, with no observable difference for implanted samples. However, new BPDs, poor surface morphology and other extended defects such as in-grown faults and hexagonal pits were observed to have formed during the annealing process. This was more severe for the samples annealed at 1850 °C and higher, and was more extensive for the implanted samples probably due to higher microwave coupling and heating of the implanted layer. The new BPDs were observed to form at the surface and create a dislocation loop that glides towards the substrate. During the high temperature annealing, the graphite cap appears to have been delaminated first in small region of the surface causing Si sublimation, which would induced strain and result in the dislocation loops. Another graphite capping process was developed and the annealing process was further optimized to protect the surface. This resulted in obtaining almost no new BPDs, while shortening or eliminating the existing BPDs.

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References:

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[3] S. Ha, et. al., Phys. Rev. Lett. 92, 175504 (2004)
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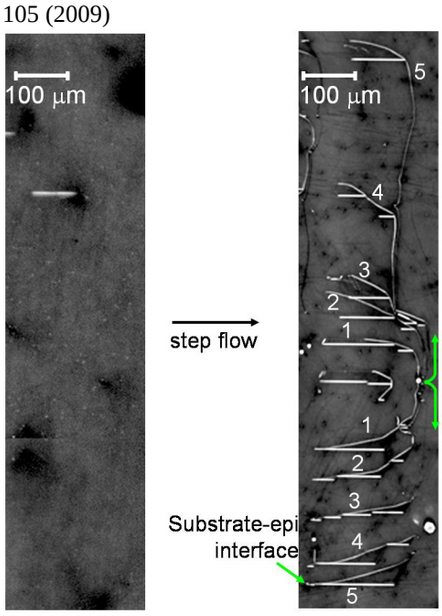

Figure 2: Dislocation loops formed at the epi surface upon annealing, which propagated towards the substrate where a misfit dislocation is formed.