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Progress in SiC MOSFET Reliability

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SiC is a unique material in that its native oxide is SiO_2 – an excellent insulator that is particularly useful in creating a field effect transistor. SiC MOSFETs have been commercially available for over two years with blocking voltage of 1200V and excellent on-state resistances (R_{DS-on}) as low as 80 mΩ. In addition, SiC MOSFETs can operate at higher temperatures than competing Si IGBTs or MOSFETs. SiC MOS technology could offer major system level efficiency improvements for motor drives, hybrid electric vehicles, photovoltaic inverters, and even grid-level applications such as flexible AC transmission systems (FACTS) (1)-(2). Currently the most significant hurdles to market penetration are reliability and cost, the latter of which is improving rapidly as the SiC technology becomes more widespread.

SiC MOSFET reliability challenges stem mainly from SiC/SiO_2 interface quality as well as interactions between devices and packaging. When operated under high gate electric field operation and high temperature, threshold voltage instabilities are often observed both in SiC MOSFET (3)-(4), and MOS capacitor (5)-(6) structures. Recent measurements on second generation commercially available SiC MOSFETs indicate significant progress on this front.

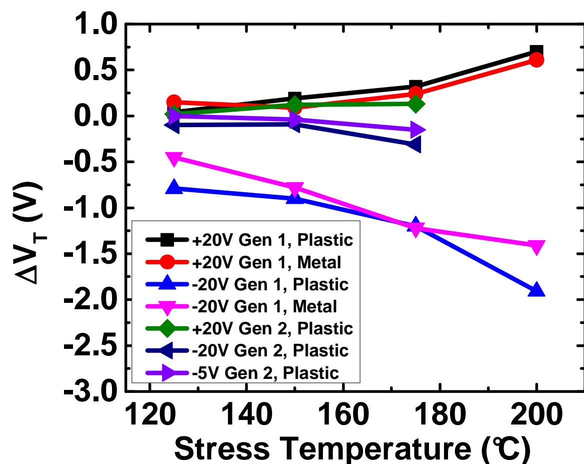

Fig. 1: V_T shift vs. temperature for Generation 1 and 2 SiC MOSFETs with stress voltage and packaging materials indicated.

In order to assess the electron and hole injection in the oxide, SiC MOSFETs were stressed with positive and negative gate voltage (V_G) for 30 min at varying temperature. Results of these experiments for first and second generation commercial SiC MOSFETs are compared in Fig. 1. V_T shifts for first generation MOSFETs (rated to 125°C) in plastic and metal packaging are plotted for gate voltages of +20V and -20V, and V_T shifts for a second generation MOSFET (rated to 150°C) in plastic packaging is plotted for V_G = +20V, -20V, and -5V (-5V is included since this is a realistic operating voltage for these parts). Each part is heated to a given temperature and allowed to settle, so the V_T shifts are plotted with respect to the measured V_T at a given temperature prior to applying gate bias stress. After each stress, the MOSFET was de-stressed by applying a gate voltage of the opposite polarity until the gate sweep matched the pre-stress curve. Both generations of MOSFETs show a larger negative shift than positive shift, indicating higher susceptibility to hole trapping than electron trapping. The second generation MOSFET shows similar shift compared to the first generation for positive gate voltage, but the shift for negative gate voltage is reduced by almost an order of magnitude. Using a gate voltage of -5V reduces this shift even further. Future experiments will include a stress that switches between positive and negative gate voltage, which is a more realistic operating condition.

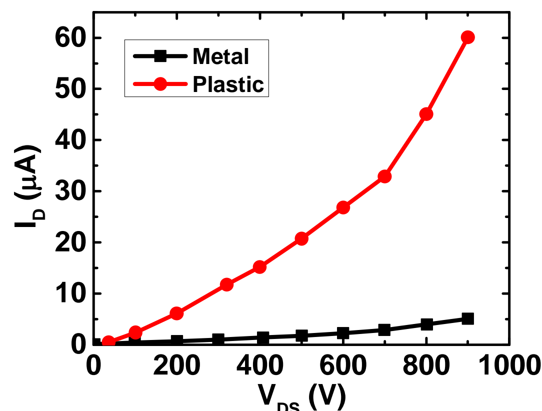

Fig. 2: V_T shifts vs. temperature for Generation 1 and 2 SiC MOSFETs

Junction leakage current at elevated temperature is compared for first generation SiC MOSFETs in plastic and metal packaging. Both show increasing leakage current at high blocking voltage as temperature increases; however, the leakage current is worse for plastic packaging, especially above 200°C. Fig. 2 plots leakage current vs. blocking voltage for plastic and metal packaged MOSFETs at 250°C with 0V on the gate. Applying a -5V gate bias significantly reduces the leakage current for metal packaging, but has no effect for plastic packaging, suggesting that there is an extrinsic leakage path in the plastic packaging. As noted above, the rated temperature for these older generation devices is 125°C, so the stress temperature is well in excess of the rated temparatuere.

Recent additional experiments demonstrate that mobility instabilities arise under certain gate stress conditions. The talk will discuss these additional results, as well as physical reasons behind the observed degradation.

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