

Multiphonon Processes as the Origin of Reliability Issues

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I. INTRODUCTION

During the last decade, advances in microelectronics have led to the aggressive downscaling of device geometries, resulting in more pronounced reliability issues. In this respect especially, the complicated behavior of bias temperature instability (BTI) has received a lot of attention [1-4]. Interesting insight into the recoverable component of BTI has been gained by a new measurement technique called time-dependent defect spectroscopy (TDDS). This new method has allowed analysis of single defects and thus helped understanding the physical trapping mechanisms behind the recoverable component of BTI. One major finding was that the BTI degradation originates from trapping of charge carriers into oxide defects. This mechanism includes non-radiative multiphonon (NMP) processes [5,6], which are also encountered in numerous related physical problems. These NMP transitions are at the heart of the multi-state defect model [1] that provides a comprehensive description of BTI and drain noise.

Increasing gate leakage is another result of downscaling and leads to unwanted heating resulting in an enormous energy consumption of MOS devices. The parasitic gate current also shows random telegraph noise (RTN), which has recently been investigated in detail [7,8]. It was found that the noise in the gate and drain currents is coupled, implying that the defects seen in BTI are also responsible for the gate current fluctuations. Interestingly, the fluctuations in the noise signal exhibit a temperature insensitive but gate bias dependent behavior, similar to direct tunneling.

II. DIRECT TUNNELING

One simple explanation for the correlated drain and gate noise may be given by a simple electrostatic picture. Therein, a charge carrier captured in an oxide defect locally repels the inversion layer, thereby reducing the direct tunneling current. At the same time, the captured charge also affects the magnitude of the drain current. These effects are visible as steps in the drain and gate current, respectively, and are correlated by the charge within the defect. This picture appears quite intuitive and seems to be further corroborated by the fact that the gate bias-dependent and temperature insensitive behavior of the direct tunneling current must be reflected in the current fluctuations of the gate noise. However, accurate state-of-the-art NEGF calculations [9] clearly demonstrate that these fluctuations reach only values below one percent of the total gate leakage current while experiments give much larger values of about 8% for pFETs or 70% for nFETs. This discrepancy rules out the electrostatic picture as a possible cause for the correlated drain and gate noise seen experimentally.

III. MULTI-STATE DEFECT MODEL

Another explanation for the correlated drain and gate noise is based on the multi-state defect model, whose

validity has been evaluated by comparison against TDDS data of pMOSFETs, including short PBTI stress pulses and dynamic NBTI stress at high frequencies. The defect in this model has a neutral (1) and a positive (2) charge state where each of them has an additional metastable state (1', 2') besides its equilibrium configuration. The actual charge transfer between the substrate and the defect proceeds via NMP processes, which are represented by the transitions $1 \leftrightarrow 2'$ and $1' \leftrightarrow 2$ in the multi-state defect model. While the former one is only involved in the hole capture and emission, the latter can explain temporary RTN and the switching behavior seen for a considerable fraction of the oxide defects.

In order to explain the observations of the correlated drain and gate noise, the existing model had to be refined: (i) In this model the gate current is due to trap-assisted tunneling (TAT), which is a two-step process from the substrate over the defect to the gate, based on NMP transitions. In order to define a current across the oxide, the state-diagram of the defect had to be extended to account for whether the tunneling hole is located in the substrate (s) or the poly-gate (p). In this generalized state-diagram, the TAT current is modeled by two consecutive NMP transitions $1_s' \rightarrow 2 \rightarrow 1_p'$. (ii) NMP processes are known to proceed over energy barriers that can only be thermally overcome. Therefore they should be temperature-activated, which is inconsistent to what is seen experimentally. Surprisingly, these processes also have a temperature independent regime if weak electron-phonon coupling with the continuum of conduction or valence band states is taken into account. In this paper, the NMP transitions and its rate expressions will be discussed in detail on the basis of parabolas and lineshape functions [10].

This refined version of the multistate model was validated against the correlated drain and gate noise data from Toledano *et al* [7]. In particular, the gate bias dependence and the missing temperature activation observed for the magnitude of the gate fluctuations can be well reproduced by the multi-state defect model. Using the same defect parameters, this model also fitted properly the capture and emission times at different gate biases and temperatures.

IV. CONCLUSION

The multi-state defect model does not only describe the charge capture and emission in RTN and the recoverable component of BTI but also gives an explanation for the gate fluctuations caused by TAT. As such, it can be regarded as a comprehensive model for reliability issues related to oxide defects.

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REFERENCES

- [1] T. Grasser *et al.*, *Proc.IRPS* (2010), pp. 16-25.
- [2] B. Kaczer *et al.*, *Proc.IEDM* (2011), p. XT.3.1-XT.3.5.
- [3] D.S. Ang *et al.*, *IEEE TDMR* **11**, 19 (2011).
- [4] V. Huard, *Proc.IRPS* (2010), pp. 33-42.
- [5] K. Huang *et al.*, *Proc.Roy.Soc.of London Ser. A* **204**, 406 (1950).
- [6] A. Palma *et al.*, *Phys.Rev.B* **56**, 9565 (2012).
- [7] M. Toledano-Luque *et al.*, *Proc.IRPS* (2012), p. XT.5.1.-XT.5.6.
- [8] C.-Y. Chen *et al.*, *Proc.IRPS* (2011), pp. 190.
- [9] O. Baumgartner *et al.*, *Proc.SISPAD* (2013).
- [10] F. Schanovsky *et al.*, *J.Comp.Electronics* **11**, 218 (2012).