Challenges for Scaled Damascene Interconnects (invited)

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Over the past two decades, the introduction of new materials and processes into the back-end-of-line portion of the IC process flow has become more and more dominant in the race for improved density and performance (Moore's Law). The main interconnects challenges are mainly located in three areas: gap fill, resistance and capacitance scaling and reliability.

This talk will mainly focus on the choice of the metallization approaches and capacitance scaling.

The efficient copper metallization of narrow lines which are used to create interconnections in damascene applications becomes more and more challenging with the decrease of the effective opening available for filling by copper electrochemical deposition (ECD). In this contribution, the 300 mm wafer copper electroplating process for damascene metallization is critically reviewed and the breakthroughs that can make this process possible are examined. Special emphasis is placed on analyzing the critical issues, such as barrier / seed options, terminal effect and future plating prospects for this technology. The smallest plateable feature size values are estimated for different metallization integration schemes, limiting the maximum sheet resistance (based on calculated and experimentally-validated terminal effect on resistive substrates) and the effective maximum filling aspect ratio to 5-6. Among the elementary steps involved in the metallization sequence, besides the achievement of a minimum-thickness/non-overhanging barrier (such as on plasma-enhanced atomic layer deposited (PEALD) Ru-based and chemical vapor deposited (CVD) MnN_x barriers), the most critical will probably be the deposition of a copper seed layer necessary to initiate the bulk copper ECD. For future generations, physical vapor deposition (PVD) techniques that are currently employed will reach a limit, as they are not able to perfectly cover the sidewalls of the narrow and high aspect ratio features. The resulting discontinuous seed layers can cause defects such as bottom voids in the copper vias and trenches. To overcome poor copper seed coverage issues, "direct on barrier" (from acid and alkaline plating solutions) and electroless copper deposition techniques (both seed formation and direct feature fill) are illustrated on 20nm half-pitch test vehicle.

Capacitance scaling, on the other hand, is achieved by introducing ultra-porous low dielectric constant materials. Nevertheless, one of the key issues in the integration of such porous materials is their inability to prevent gaseous penetration, e.g. during the metallization. Several strategies are being followed to minimize the processing damage to the porous films during etching and ashing. The next important step is to seal the pores at the surface, especially at the sidewalls after the trench and via etching. This is to prevent metal or precursor penetration during the metallization process, especially by advanced conformal deposition techniques such as CVD and ALD. There are several routes to sealing: i) by thin film deposition; ii) by plasma-surface interaction; iii) by surface cross-linking/reconstruction. In this contribution, we report about the achievement of a complete pore sealing by combining a surface treatment of the low-k material together with Self-assembled monolayers (SAMs) deposition and a low temperature ALD and CVD processes.

Key words: damascene interconnects, copper, electroplating, electroless deposition, self-assembled monolayers, porous-low k materials, pore sealing.