Fin Doping by Hot Implant for 14nm FinFET Technology and Beyond

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The transition from a planar to a FinFET device structure has changed device doping requirements [1]. The depth control for USJ for planar devices is no longer relevant with FinFETs, but fin sidewall doping and activation, junction profile and leakage control, and crystallinity control of the fin become new challenges. The energetic ions from implants can cause crystalline damage to the fin and increase junction leakage and fin parasitic resistance. With continuous scaling of FinFET technology, the fin width decreases in each technology node. The smaller fins become more prone to damage by ion implant. We have demonstrated for the first time that hot implant for SDE on 6nm CD vertical fin produced single crystalline fin and enabled 5X improvement in fin line resistance and more than 10X reduction in junction leakage compared with a room-temperature SDE implant.

Advantages of ion implant for FinFET doping are precision dose and energy control, which enable precision tuning of transistor performance and reduced device variability. Ion implant can lead to amorphization of the Si fin. The amorphization is the result of a critical balance between damage generation and its annihilation [2]. It has been shown that shallow angled implants at room temperature can amorphize a narrow fin [3] and lead to incomplete regrowth during the activation anneal. We have introduced hot implant to solve this problem and results were validated by fin resistor testing and TEM. The process flow and structure layout for the fin resistors are shown in Figures 1and 2. The fins were implanted with hot and room temperature SDE implant at low energy and high dose, followed by a spike anneal for dopant activation. The fin line resistance and junction leakage are shown in Figures 3 and 4. Below a threshold at about 15nm where the RT implanted fin become polycrystalline, hot implant improved conductance by 5x and junction leakage by >10x..

For high dose implants such as SDE implant, the energetic ions damage the Si crystal lattice and amorphize the surface region. TEM characterization showed that a room temperature implanted fin at 12nm CD was completely amorphous and that a 30nm CD fin had a 7nm amorphous outer-layer, (Figure 5a and 5b.) After spike anneal the narrow fin became polycrystalline and the wide fin was single crystalline with visible defects, shown in 5c and 5d. The crystallinity of the narrow fin could not be restored during anneal due to the Si single crystal seed located in the substrate far away from the top portion of the fin during SPE growth. For the wide fin, the inner crystalline core served as seed for recrystallization during anneal and led to recovery of fin crystallinity. In comparison, a hot implanted 6nm fin was single crystalline (Figure 6.) The critical implant dose for the amorphization transition in Si is a function of implant temperature [4]. Increasing the implant temperature enhances the dynamic annealing and increases the critical dose needed for Si amorphous layer formation. The free surface on the fin also serves as sink for point defects. The reduction of defects improved junction leakage and reduced parasitic resistance. Hot implant changes the amount of de-channeling and defect formation. By using hot implant, substrate amorphization is reduced resulting in a deeper profile. Hence the implant energy may need to be reduced to match the RT implant profile.

High energy low dose As halo implants were also carried out. Defect pockets were seen on a narrow fin after room temperature halo implant, and the fin had defects after spike anneal, (Figure 7a and 7b.) Figure 8 shows an 8nm narrow fin after hot halo implant that was single crystalline. Hot implant is shown to be an effective mechanism to control implant damage and optimize the doping level in very low CD FinFET structures.

Figure 1. Fin process flow

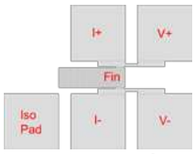

Figure 2. Fin resistor layout

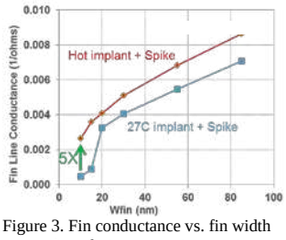

Figure 3. Fin conductance vs. fin width comparison hot vs. room temperature implant

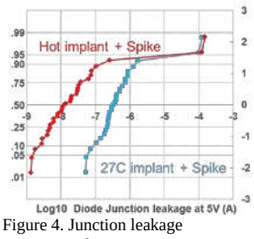

Figure 4. Junction leakage comparison hot vs. room temperature implant

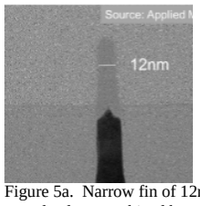

Figure 5a. Narrow fin of 12nm CD completely amorphized by room temperature As SDE implant

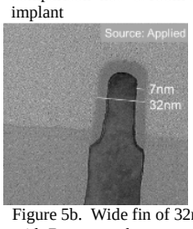

Figure 5b. Wide fin of 32nm CD with 7nm amorphous outerlayer post room temperature SDE implant

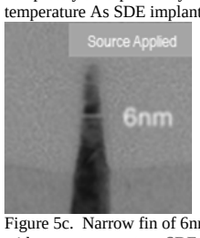

Figure 5c. Narrow fin of 6nm CD with room temperature SDE implant was polycrstalline after spike anneal

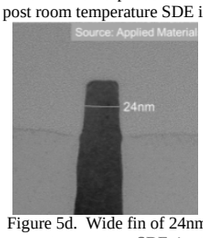

Figure 5d. Wide fin of 24nm CD with room temperature SDE implant was single crstalline after spike anneal

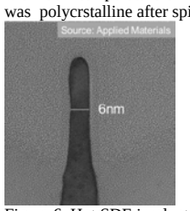

Figure 6. Hot SDE implant produces single crystalline 6nm fin

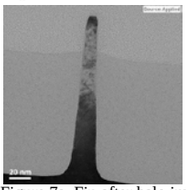

Figure 7a Fin after halo implant at room temperature

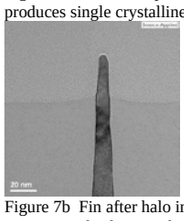

Figure 7b Fin after halo implant at room and split anneal

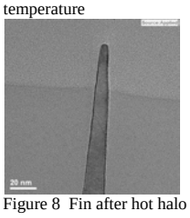

Figure 8 Fin after hot halo implant

Ref. [1] C. Auth et al., pp.131, VLSI proceeding 2012
[2] L. Pelaz, et al., J. Appl. Phys. 96, 5947 (2004),
[3] Duffy et al., Appl. Phys. Lett. 90, 241912 (2007)
[4] Morehead et al., J. Appl. Phys. 43, 1112 (1972)