Abstract #2189, 224th ECS Meeting, © 2013 The Electrochemical Society

Advanced physical characterization of Si-passivated III-V semiconductors for low-power logic applications: Defect chemistry, band bending and surface photo-voltage

C. Marchiori[1], M. El-Kazzi[1*], L. Czornomaz[1], D. Pierucci[2], M. Silly[2], F. Sirotti[2], S. Abel[1], E. Uccelli[1], M. Sousa[1], J. Fompeyrine[1]

[1]IBM Research GmbH– Zuerich Laboratory, Säumerstrasse 4, 8803 Rüschlikon, Switzerland
[2] Synchrotron SOLEIL, L'Orme des Merisiers, 91192 Gif-Sur-Yvette Cedex, France
* Currently at Paul-Scherrer Institute (PSI), Villigen, Switzerland

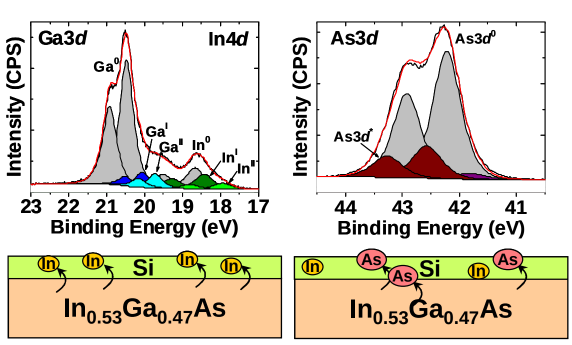
Replacing Si as a channel material in future metal-oxide-semiconductor field effect transistors (MOSFET) is today the leading option for advanced CMOS technology nodes. For n-FET, $In_{0.53}Ga_{0.47}As$ (InGaAs) offers the best compromise between electron mobility and band-gap.

Over the last years, important progress has been made in the development of InGaAs based MOSFETs for future low-power logic application. Devices with promising characteristics have been reported. Integration path for self-aligned, laterally scaled devices has been shown [1]. Fabrication of similar devices on silicon substrate has been also demonstrated, for example using the transfer of high-quality, thin III-V heterostructures onto Si by direct wafer bonding [2]. Understanding and controlling the density of interface states (D_{it}) between the InGaAs channel and the gate dielectric remains however a key issue to obtain competitive device characteristics with respect to Si based devices.

An appropriate gate dielectric is characterized by three different metrics, namely i) a low capacitance-equivalent thickness (CET<1.3nm) with low enough leakage current, ii) $D_{it}<10^{12}cm^2$ and iii) a thermal stability compatible with a gate first or gate last integration flow.

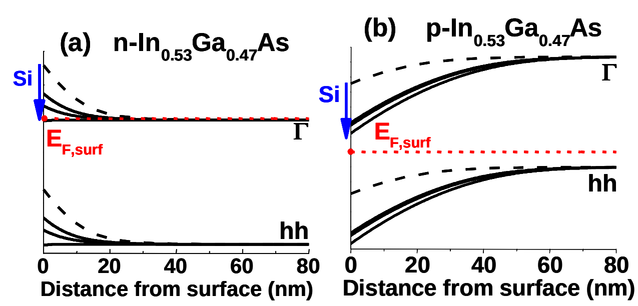
Using thin, passivating layers of amorphous Si onto InGaAs, sub-1.5nm CET MOS capacitors and FETs with excellent mobilities have been demonstrated [3,4], in particular using a gate first integration flow. Better performance would require however to further reduce D_{it}. A detailed understanding of critical instabilities intimate to the physics and chemistry of the α-Si/InGaAs interface is therefore required. By combining laboratory and synchrotron X-ray photoelectron spectroscopy (XPS) data, we describe 1) the interface formation from the initial sub-monolayer reaction, 2) the evolution of its chemical composition, 2) Si-induced band bending and specific defect states in the InGaAs band gap, 3) surface photo-voltage effects on clean and Si-reacted interfaces.

The figure below summarizes two key features observed in the surface chemistry of InGaAs channels

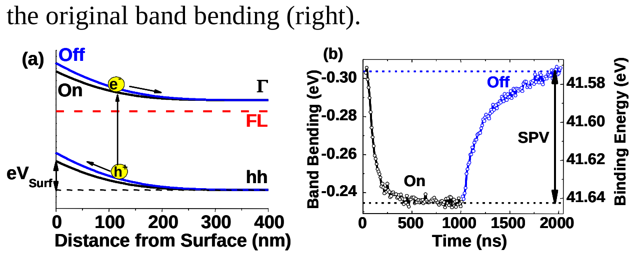


exposed to Si deposition. First the evolution of Ga3*d* and In4*d* core levels upon Si deposition is reported in the right figure. Each core level is featured by a doublet: Ga3$d_{5/2}$ and Ga3$d_{3/2}$, In4$d_{5/2}$ and In4$d_{3/2}$. Ga3d^0, In4d^0 are bulk doublets, while Ga3d^I, Ga3d^{II}, In4d^I and In4d^{II} are Si-induced components. The observation is consistent with an inherent instability between α-Si and InGaAs, leading to slight out-diffusion of Indium atoms. This phenomenon takes place starting from Si thicknesses as low as 0.3nm. In addition, the evolution of the As3*d* doublet upon 380ºC anneal in UHV (left figure) reveal that this additional thermal treatment triggers a small out diffusion of arsenic. (As3d^0 is bulk doublet, As3$d^*$is Si-induced component).

Simultaneously, the evolution of band bending can be extracted from the XPS data as illustrated in the figures below. The evolution upon Si deposition is schematized for both n- and p-type samples, respectively. With respect to the clean samples, Si deposition flattens the bands in n-type whereas an increased bending is induced in the opposite direction, creating surface inversion in p-type $In_{0.53}Ga_{0.47}As$. This observation seem to indicate that the deposition of Si onto the $In_{0.53}Ga_{0.47}As$ surface does not completely "un-pin" the Fermi level, in the sense that interface states are not eliminated. In the latter case, flat band condition should be observed for all samples.



Finally, time resolved surface photo-voltage (SPV) experiments are performed to gain additional insight. In this pump-probe experiment, $In_{0.53}Ga_{0.47}As$ samples are excited using a pulsed laser (λ = 405 nm). Laser-induced band bending variation are followed by recording core level spectra. The mechanism depicted in the figure below (left) has been widely reported for Si. Electron-hole pairs photogenerated in the space charge region are quickly separated by the strong electric field: for upward (downward) band bending, holes (electrons) are swept towards the surface. This decreases the negative (positive) charge density trapped in the surface states and *reduces* the original band bending (right).



From these different observations, a consistent description of the interface defect chemistry between a-Si and InGaAs can be proposed, paving the way to solutions to further improve the quality for device operation.

[1] L. Czornomaz et al., Proc. 2012 70th DRC (2012)
[2] L. Czornomaz et al., IEDM Tech. Dig. (2012)
[3] M. El Kazzi et al., APL **100**, 063505 (2012)
[4] M. El Kazzi et al., APL **99**, 052102 (2011)