Source & Drain Contact Module for FDSOI MOSFETs

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The Fully Depleted Silicon On Insulator (FDSOI) technology has become a credible alternative to the bulk one for the 28 nm node and below: it indeed exhibits several advantages such as very good electrostatic control and low variability [1]. The scaling of FDSOI devices is associated to a global reduction of device dimensions: body thickness, gate length, contacted gate pitch, distance between the source/drain contacts and the gate. Due to the reduction of contact areas, the contact resistance in the source & drain regions between the metal and the semi-conductor appears as the main contributor to the global access resistance [2]. It is thus essential to carefully optimize the contact module to fully benefit from the high potentialities of the FDSOI technology.

The most popular approach to contact simultaneously the gate and the sources and drains is the Self-Aligned Silicidation process (SALICIDE process) [3]. Thanks to its low resistivity, low Si consumption and low formation temperature, Ni-based silicide (NiSi) has been introduced in mass production from the 65nm node [4]. However, its integration in FDSOI devices is challenging due to the specificities of these architectures. In particular, various strain engineering options are envisaged to boost carrier mobility including tensely Strained SOI substrates (sSOI), SiGe channels, raised SiGe or Si:C sources and drains etc [5-8]. Thus, the salicidation must be carefully tuned in order to achieve a thin, uniform and stable silicide film with a suitable contact resistivity on each material. Moreover, it must be compatible with strain engineering approaches. Indeed, the role of SiGe (for pMOS) or Si:C (for nMOS) sources and drains is to induce some uniaxial strain in the channel, thereby enhancing the mobility. When the solid state reaction between the metal and the semi-conductor is not tailored properly with respect to metal thickness and annealing conditions, a degradation of the underlying epitaxial layer can be observed, as illustrated for SiGe:B in fig. 1. Consequently, the strain in the channel may be strongly reduced (fig. 2) [9].

In this paper, various aspects of the salicide process for sub-28nm FDSOI devices will be presented concerning the metal deposition specifications (thickness, metal alloys), thermal treatments, wet etching step and process-induced strain behavior. A focus will be put on the morphological stability of the silicide layer. This point needs to be addressed especially when the metal reactive diffusion is performed on SiGe. Indeed, Ni germanosilicide films suffer from morphological degradation caused by Ge segregation – induced agglomeration [10, 11]. To overcome this issue, NiPt alloys with few percents of Pt have been successfully introduced in Si and SiGe devices [12]. The use of Pt appears now mandatory. However, it increases the complexity of the solid state reaction mechanisms and requires in-depth investigations (phase sequence, kinetics, Pt role on Ge segregation) which will be discussed.

Finally, we will propose some orientations to achieve a robust source & drain contact module compatible with sub-28nm FDSOI technology nodes.

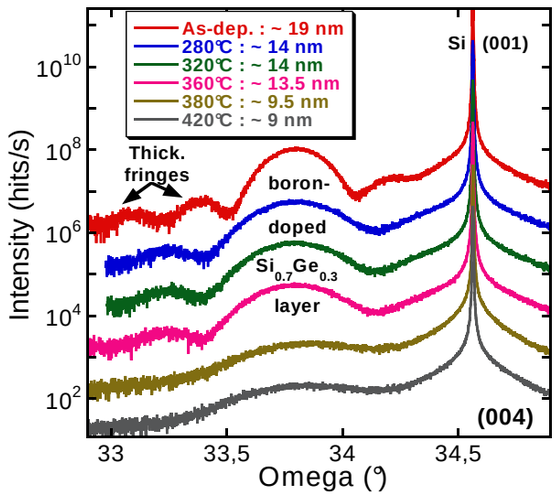

Fig.1. High Resolution Ω/2θ scans around the (004) XRD order for 7nm of NiPt (5% of Pt) deposited on 19nm of epitaxial in situ boron doped $Si_{0.7}Ge_{0.3}$ layers. Red curve on top: as deposited Ni(Pt) reference. Bottom curves: samples annealed at 280°C, 320°C, 360°C, 380°C and 420°C for 30s in N_2 ambient. SiGe:B thicknesses still diffracting coherently after silicidation are provided in the graph.

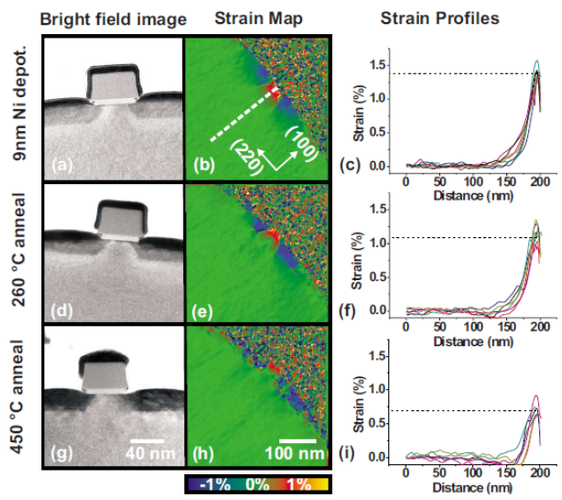

Fig.2. Bright-field TEM image, a (220) strain map, and profiles extracted from the region indicated by the dashed line in (b) for a SiGe device with a Ge content of 35% after different stages of the silicidation process. (a), (b), and (c) correspond to as-deposited reference of 9nm of Ni(Pt) with 5% of Pt ; (d), (e), and (f) are as above after a 260 °C anneal. (g), (h), and (i) correspond to the specimen after a 450 °C anneal [11]

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