Nanoscale Heterogeneous Reactions and Interfaces in Ge/Si and for III-V on Si Integrated Devices

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In the pursuit of realizing sub-10 nm transistor channel lengths in homogenous and heterostructured materials, nanoscale defects and hetero-interfaces can significantly impact the formation of alloyed metal contacts conventionally used in CMOS devices. Similar reactions to those involved in the formation of such contacts can in turn be tailored to integrate III-V materials to Si, in various forms and dimensions, in a top-down CMOS compatible process.

We utilize in-situ transmission electron microscopy to unveil new observations on the detailed formation of such alloys and interfaces at an atomic scale by capturing single nucleation events during the reaction of Ni with Si, Ge and Ge/Si core/shell nanowires. While homogenous nucleation in Ni_xSi and Ni_yGe nanowires is favored,[1] heterogeneous nucleation at crystalline *surface* grains and stacking faults, as well as at *body* twin boundaries,[2] which may arise during epitaxial regrowth, becomes dominant and modify the source/drain interface profile and posing limits to the shortest achievable channel lengths. The reaction in heterostructured Ge/Si core/shell nanowires advances with disproportionate extensions, typically with Ni_yGe lagging behind Ni_xSi. We have developed a process that allows simultaneous advancement of both fronts in heterostructured Ge/Si core/shell nanowires and achieved channel lengths as short as 2 nm in a Ge/Si core/shell nanowire.[3]

In bulk and on planar surfaces, the reaction between Ni and Si is well controlled and understood. We have utilized this reaction to integrate dielectric-capped InGaAs layers to Si and fabricated InGaAs FinFETs directly on Si for the first time.[4] The heterogeneous integration process was implemented on either flat Ni layers or on patterned Ni electrodes. When the underlying Si substrate was capped with a dielectric layer and patterned Ni leads were deposited atop, the reaction between Ni and InGaAs have resulted in direct wafer-bonded and self-aligned InGaAs channels on dielectric on Si.

This paper will overview fundamental material science aspects relevant to these hetero reactions and interfaces and discusses their transport properties and the opportunities they offer.

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