PN-Diode P-Oxide-Semiconductor/N-SiC/N-Si Resistive Nonvolatile Memory for Cross-Point Memory Array

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Recently, we have proposed pn-diode p-oxide-semiconductor/n-SiC/n-Si resistive nonvolatile memory which has a rectifying *I-V* characteristic and suitable for ultimately high-dense memory array with a cross-point memory cell configuration. For this type of memory, we have proposed p-AgO_x/SiO_x/n-SiC/n-Si(111) (hereafter called type A) and p-CuO_x/SiO_x/n-SiC/n-Si(111) (hereafter called type B) devices on the basis of our previously proposed metal-insulator-semiconductor (MIS) memory devices [1-3]. In this paper, we report their fabrication processes, and thier memory function chracteristics and mechanisms.

In these devices, we formed 80-100 nm n-type SiC layers on 0.1-0.2 Ω cm 4˚ off-axis n-Si(111). SiO_x layers were formed by thermal oxidation of n-SiC surfaces. P-type AgO_x and CuO_x oxide semiconductors were formed by oxidation of 50-150 nm Ag and Cu layers. We show the layer structures of these devices in Fig. 1.

In Fig. 2, we show typical *I-V* curves obtained from (a) type A and (b) type B devices. To investigate the roles of SiO_x and SiC layers, we also prepared (c) p-AgO_x/SiO_x/n-Si(111) device, where SiC is absent, and (d) p-CuO_x/n-SiC/n-Si(111) device, where SiO_x is absent. The type A (curve (a)) and B (curve (b)) devices exhibit excellent rectifying *I-V* curves and in the forward positive bias, they exhibit hysteresis characteristics, that is, memory functions where a high resistance (off) state transitions to a low resistance (on) state. However, in curves (c) and (d), no hysteresis was observed, indicating that SiO_x formed by oxidation of SiC is related to generation of hysteresis in the forward bias.

Fig. 3 shows a typical *C-V* curve obtained from the type A device, and a similar *C-V* curve was also obtained from the type B device, indicating that the hysteresis is caused by negatively charged electron traps. The trap states probably correspond to the SiO_x defect states. In Fig. 4, we illustrate the expected device memory functions. When electrons are trapped at the defect states, the device becomes an off state ((1) and (4)), and when the defect states are empty, the device becomes ((2) and (3)) an on state. The devices response in the order of microseconds to the erase, write, read input voltages and their endurance switching cycles are more than 10^5 times.

In conclusions, we demonstrate pn-diode type resistive nonvolatile memory devices where electron trap states are sandwiched p-type oxide semiconductor and n-type semiconductor. They exhibit excellent rectifying *I-V* characteristics and low and high currents are switched in the forward bias by transferring electrons into and from the trap states. The rectifying behavior is suitable to ultimately high-dense cross-point configuration array.

REFERENCES

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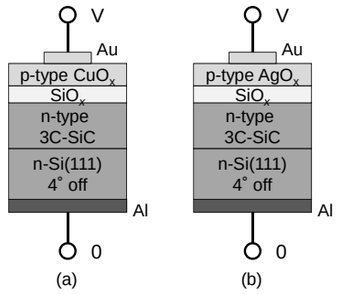

Fig. 1. Layer structures of our proposed (a) p-CuO_x/SiO_x/n-SiC/n-Si(111) and (b) p-AgO_x/SiO_x/n-SiC/n-Si(111) resistive nonvolatile memory cell.

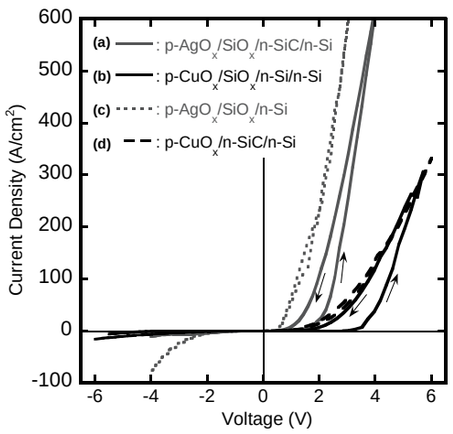

Fig. 2. Typical *I-V* curves obtained from (a) p-AgO_x/SiO_x/n-SiC/n-Si(111), (b) p-CuO_x/SiO_x/n-SiC/n-Si(111), (c) p-AgO_x/SiO_x/n-Si(111), and (d) p-CuO_x/n-SiC/n-Si(111) layer structure devices.

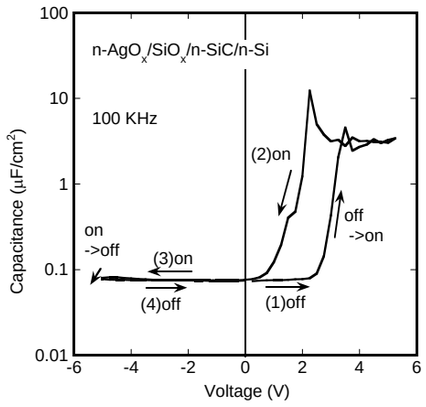

Fig. 3. Typical *C-V* curve obtained from our proposed p-AgO_x/SiO_x/n-SiC/n-Si(111) memory.

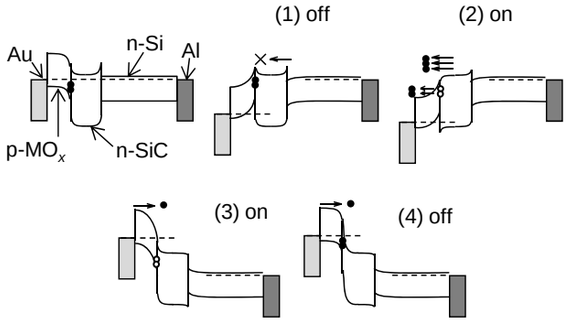

Fig. 4. Expected memory function mechanisms for our proposed pn-diode memories using p-MO_x/SiO_x/n-SiC/n-Si(111) memory band diagrams assuming MO_x is Ag_2O.