Reliability of La-silicate MOS capacitors with tungsten carbide gate electrode

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Reliability of La-silicate gate dielectrics with tungsten carbide gate electrode have been investigated by Time Dependent Dielectric Breakdown (TDDB) method. During constant voltage stress of the MOS capacitors, La-silicate MOS capacitors with tungsten carbide gate electrodes show better reliability due to the nice interface properties.

Continued scaling of gate oxide thickness in CMOS has caused the quality and reliability issue of ultrathin dielectrics [1]. It is therefore important to investigate the reliability of gate dielectrics. La-silicate gate dielectrics are regarded as promising candidates for gate dielectric materials for further equivalent oxide thickness (EOT) scaling [2]. In this work we investigate the reliability of La-silicate, the metal gate has been adopted tungsten carbide, which known as refractive compound metal and it can improve the interface properties of La-silicate MOS capacitors [3].

MOS capacitors were fabricated on *n*-Si (100) substrates. After performing SPM and HF chemical cleanings, we conducted deposition of thin La_2O_3 gate dielectric films by e-beam evaporation at a substrate temperature of 300°C. Tungsten and carbon multi-stacking layers with total thickness of 10 nm were deposited by RF magnetron sputtering. TiN (10 nm) and Si (100 nm) capping layers were deposited on W/C metal also by RF sputtering to control the silicate reaction [4]. The samples were annealed at 800°C in N_2 ambient. Back side contacts were formed by Al deposition. Finally, the sample was annealed in forming gas (N_2:H_2=97:3) ambient at 420 °C for 30 minutes. Fig. 1 shows the whole fabrication process.

Fig. 2 shows C-V characteristics of capacitors with W_2C gate electrode, where W gate electrode is shown as a reference. Interface state densities measurement by conductance method revealed smaller value with eliminating the hump in the C-V curve. Moreover, the flatband voltage showed a shift to positive direction, indicating reduction in positive fixed charges. Fig.3 shows interface state density (D_{it}) versus stress time plot on different stress bias (V_{st}=2.0 V, 3.0V). Interface state density increase with increasing of stress voltage for both case, indicating electron trapped state generated La-silicate dielectrics, but W_2C gate electrode effectively suppress the D_{it}.

In conclusion, reliability of La-silicate has been found to be improved by W_2C gate electrodes.

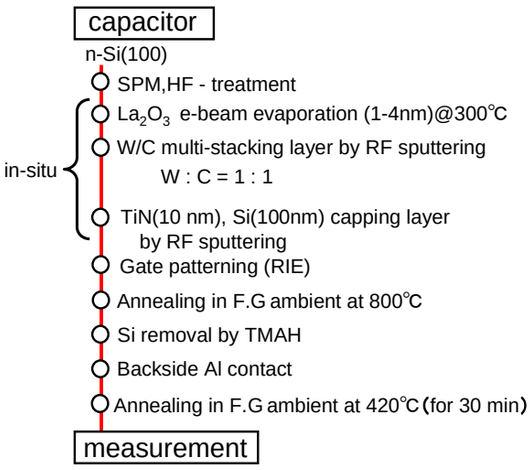

Fig. 1 Device fabrication process

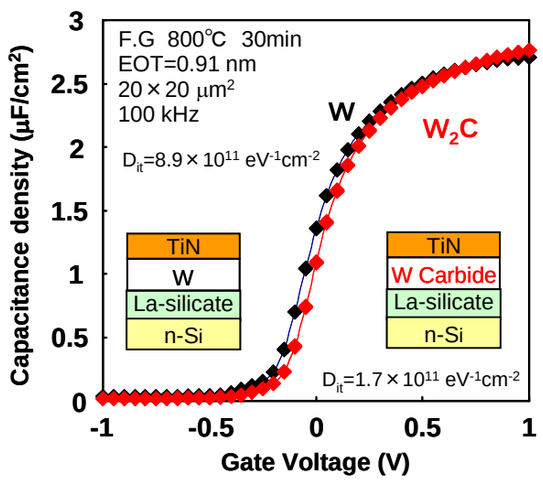

Fig. 2 C-V characteristics of TiN/W_2C/La-silicate /*n*-Si and TiN/W/La-silicate/*n*-Si capacitors

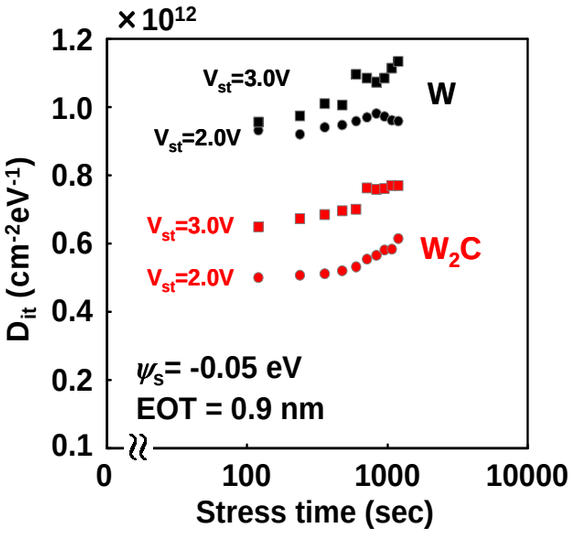

Fig. 3 Interface state density (D_{it}) versus stress time plot on different stress bias

References

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