Lateral Nonuniformity of the Tunneling Current of Al/SiO_2/p-Si Capacitor in Inversion Region due to Edge Fringing Field Effect

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Interesting area dependency (AD) and perimeter dependency (PD) mechanisms of dark gate current in Al/SiO_2/p-Si capacitor is shown in Fig. 1. The areas of Sample S, M, and L are $1\times2.25\times10^{-4}$, $4\times2.25\times10^{-4}$, and $16\times2.25\times10^{-4}$ cm^2 and the corresponding perimeters are $1\times6\times10^{-2}$, $2\times6\times10^{-2}$, and $4\times6\times10^{-2}$ cm. The left ordinate axis of Fig. 1 shows the gate current value per unit area (I_G/A) and the right ordinate axis shows the gate current value per unit perimeter (I_G/P). When the MOS capacitor biased at negative voltage, the I_G/A will overlap together well, here defined as AD region. When the negative bias decreases, after passing the change of oxide band bending direction, these three I_G/A begin to diverse; on the contrary, I_G/P begin to merge together. At the positive biased region, the gate current is dependent on gate perimeter but not area, and defined as PD region.

In order to study the effects of gate area and gate edge, we intentionally design three different thicknesses of top gate aluminum (250, 6, and 3 nm). Besides, the skin depths of aluminum in the visible spectrum are 3~4 nm. That is, if the thickness of aluminum beneath 4 nm, the top aluminum gate will be a bad conductor and we expect it will be pervious to light. Fig. 2 is the I_G of MOS(p) capacitors with different thicknesses of top gate aluminum and the oxide thickness is 2.1 nm. The dark currents of 250nm- and 6 nm-Al capacitors are almost the same. However, the dark current in inversion region of 3 nm-Al capacitors increases unusual. That is because of the bad conductor, 3 nm-Al top gate. When the probe (smaller than the gate pattern) was applied to the gate, the different gate areas sustained different gate voltages. The place which was distant from the probe would endure smaller gate voltage due to larger sheet resistance. At this time, the area beneath the probe would enter deep depletion region first, and be lack of minority carriers. And other area which was still in inversion region will provide electrons to reach charge neutrality and therefore induce extra current as observed in Fig. 2.

Fig. 3(a) is the I_G of MOS(p) capacitor with oxide thickness of 2.1 nm under illumination of 20, 30, and 40 mW/cm^2. It is clear that, the saturation current could be enhanced with the increasing of density of photo-illumination. This result is attributed to the enhanced edge deep depletion absorption of light due to edge fringing field effect. The structure of MOS(p) capacitor exhibits an enhanced edge charge collection characteristic that could be applied to generate the considerable photocurrent in magnitude. Fig. 3(b) is the I_G of MOS(p) capacitor with different thicknesses of top gate aluminum of 250, 6, and 3 nm after light illumination. The intensity of light is 20 mW/cm^2. After 20 mW/cm^2 illumination, the currents will be enhanced obviously with the decreasing of the thickness of aluminum. That is because the characteristic of pervious to light of gate area with thinner aluminum gate.

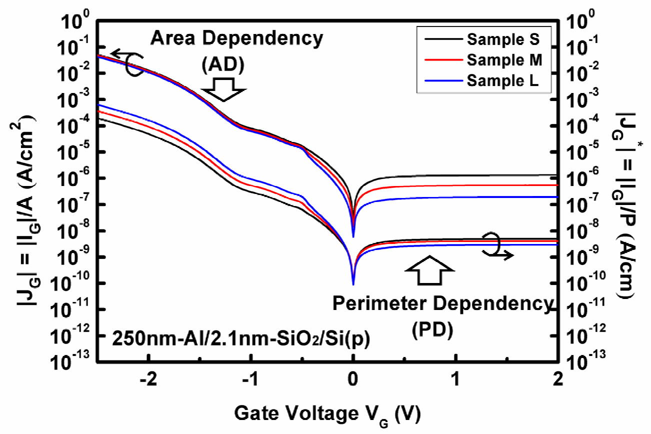

Fig. 1 The $|I_G|/A$ and $|I_G|/P$ versus gate voltage of MOS(p) capacitors with different gate electrode areas but the same oxide thickness of 2.1 nm. The measurement is carried out in the dark.

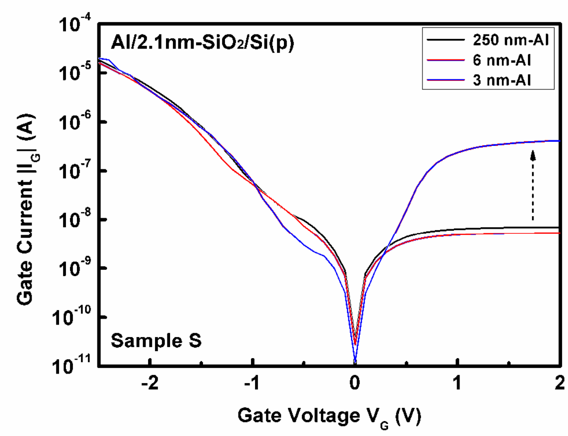

Fig. 2 The gate current $|I_G|$ of MOS(p) capacitors with different thicknesses of top gate aluminum of 250, 6, and 3 nm. The oxide thickness is 2.1 nm. The measurement is carried out in the dark.

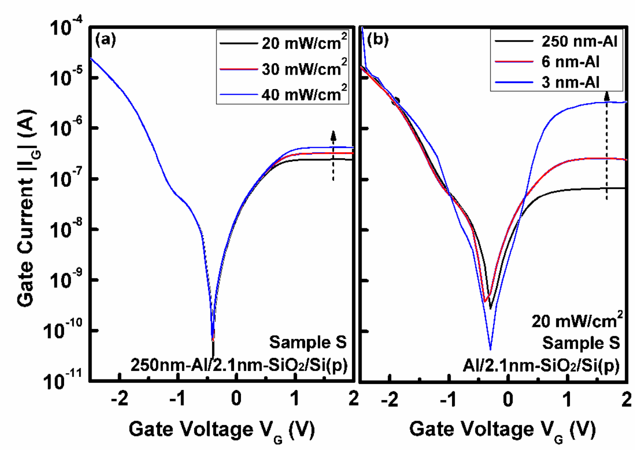

Fig. 3(a) The gate current $|I_G|$ of MOS(p) capacitors under illumination of 20, 30, and 40 mW/cm^2. (b) The $|I_G|$ with different thicknesses of top gate aluminum of 250, 6, and 3 nm after light illumination. The intensity of light is 20 mW/cm^2. The oxide thickness is 2.1 nm.