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ALD W CMP characteristic for HKMG integration

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When scaling CMOS devices to 45 nm and beyond, high-k/metal gate (HKMG) stack is needed based on the considerations such as reducing gate tunneling current and gate resistance and eliminating the depletion effect in polycrystalline silicon, etc.[1,2]. Gate last integration scheme had become a mainstream because it ensures the thermal stability of high-k and metal gate stack by applying the metal gate after the high temperature source/drain activation anneal [3]. During HKMG gate last CMOS integration, metal gate chemical and mechanical planarization (CMP) is an indispensable and key process step. Al metal gate is firstly introduced from 32nm node by Intel, which brought new process challenges for Al filling and correspondent CMP [4]. Our groups are attempting to adopt W as metal gate using atomic layer deposition (ALD) method, besides of ALD W ideal fill capability, compatibility with traditional W CMP is also taken into account. In this work, CMP behaviors were examined for different types ALD W in order to provide references for exploring W metal gate CMP process.

Fig. 1 gives SEM morphology of ALD W layer using SiH_4 and B_2H_6. Different morphology and crystalline state was observed. Fig. 2 gives XRD patterns of ALD W layer using SiH_4 and B_2H_6. It can be seen that SiH_4 base ALD W is polycrystalline, while B_2H_6 base ALD W is amorphous, which was consistent with corresponding SEM results. The same W CMP process conditions were used to check ALD W removal rate (RR). Fig. 3 gives the ALD W RR chart after normalized. The ALD W RR with B_2H_6 base was faster about 2 times than that of SiH_4 base. The big RR difference should be attributed to the different crystalline state. Compared with polycrystalline SiH_4 base ALD W, amorphous B_2H_6 base ALD W may be easy to oxidization in acidic W slurry environment. Table I gives surface RMS of ALD W layer pre and post CMP within 10 μm x 10 μm. The surface topography of B_2H_6 base ALD W was relatively smoother than that of SiH_4 base. RMS of ALD W post CMP were all smaller 1nm.

In conclusion, CMP behavior was examined for ALD W with SiH_4 and B_2H_6 base. Crystalline state of ALD W for SiH_4 and B_2H_6 is respectively polycrystalline and amorphous. B_2H_6 base ALD W has quicker CMP RR than that of SiH_4 base. RMS of ALD W post CMP were all smaller 1nm for with SiH_4 and B_2H_6 base.

References

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[3] K. Mistry, et al., Electron Device meeting, IEDM, 247 (2007)
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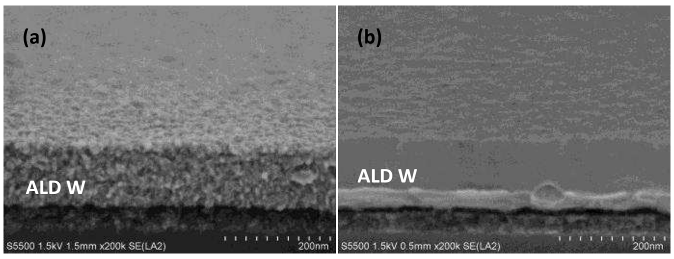

Fig. 1 SEM morphology of ALD W layer (a) SiH_4 base (b) B_2H_6 base

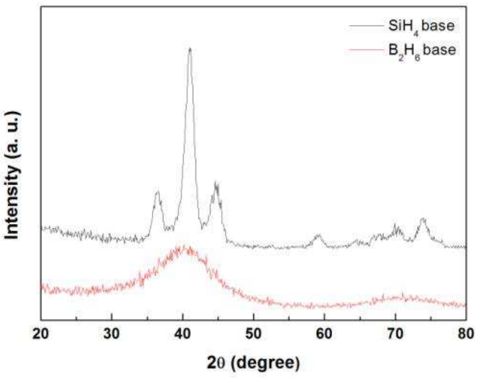

Fig. 1 XRD patterns of ALD W layer using SiH_4 and B_2H_6

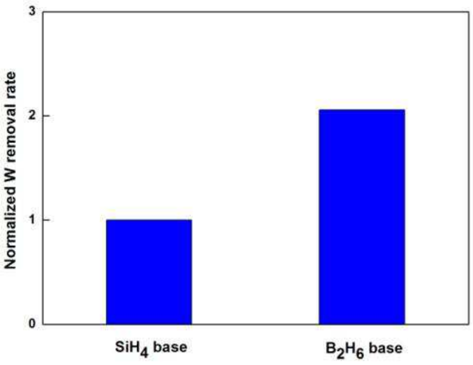

Fig. 3 Normalized ALD W removal rate chart

Table I. Surface RMS of ALD W layer pre and post CMP within 10μm x 10μm

ALD W conditions	pre CMP	post CMP
SiH4 base	1.16 nm	0.73 nm
B2H6 base	0.94 nm	0.3 nm