Resistivity of Ni silicide nanowires and its dependence on Ni film thickness used for the formation

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Resistivity of Ni silicide nanowires (NWs) formed by 2-step annealing process have been measured by four-point method. It was found that the resistivity depends on the wire width as well as the thickness of the Ni thin film used for the silicide formation. There is an optimum Ni thickness for obtaining the smallest resistivity for all NW width. The film thickness dependence may mainly be caused by difference in Ni silicide phase, due to Ni/Si amount ratio change before the silicidation.

Ni silicidation has been widely used to reduce the parasitic resistance at source and drain regions of MOSFETs and this technology will continue to be used for highly scaled devices. One of the concerns of Ni silicides is their resistivity increase with the scaling, when applied to Si nanowire FETs. In this paper, in order to reduce resistivity of narrow wires, Ni thickness dependence of the Ni silicide NW resistivity was intensively investigated.

Ni silicide nanowires were formed by the reaction of Ni films (thickness 7, 10, 80 and 120 nm) and Si fin patterns with width ranging from 20 to 90 nm. The Si fins were formed by the RIE of SOI layer and the height of fin was 30 nm for all line widths. Silicidation was conducted at annealing temperatures of 270 °C (RTA1, 2min) and 500 °C (RTA2, 1min). Before the RTA2, unreacted Ni layer was removed. Resistances of wires were measured by four-point method with TiN electrodes aligned on Ni silicide wires. Figure 1 shows a SEM image of a fabricated device. The measurement line length was varied from 3 to 6μm and the resistivity of the silicide was extracted from the slope of the length dependence.

Figure 2 shows that resistivity dependence on the NW width. Ni thickness was taken as a parameter. Ni silicide resistivity increased for NW width less than 40nm for Ni thickness more than 10nm. This trend was similar to the previous result [1], however the increase was suppressed to a little more than 50μΩcm when thin Ni (10nm) was used for the silicidation. Stable and lowest resistivity was also obtained for 10nm Ni for NW width more than 40nm (about 20 μΩcm). Appropriate Ni/Si amount ratio may lead to the formation of low resistivity silicide phase such as NiSi or Ni_2Si in this width range. For thinner Ni thickness (7 nm), however, the drastic increase in the resistivity was observed. This may be due to the Ni silicide agglomeration because the formed Ni silicide was extremely thin [2]. Figure 3 shows the resistivity as a function of the Ni thickness. The NW with was taken as a parameter. This figure clearly indicates that the thickness around 10nm is an optimum for this Si fin height and the silicidation condition.

In conclusion, resistivities of Ni silicide nanowires formed by 2-step annealing process have been measured by four-point method. By controlling the thickness of Ni film, drastic increase of the resistivity at narrow wire was suppressed. Controlling the Ni/Si amount ratio is important for obtaining the low resistivity Ni silicide NWs.

References
[1] K. Matsumoto et al., Proceedings of the 2nd International Symposium on Next-Generation Electronics (**ISNE 2013**), Kaohsiung City, Taiwan.
[2] Ting-Hsuan Chen et al., ECS Journal, 1(2) P90-P93 (2012).

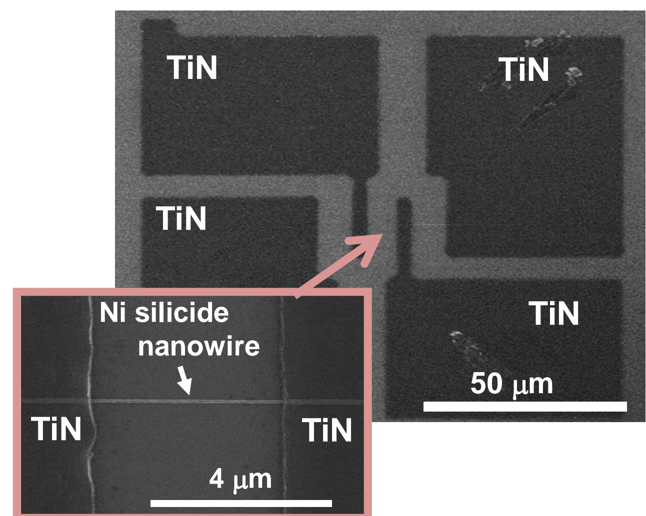

Fig.1: SEM images of a Ni silicide nanowire and four point measurement setup with TiN electrodes.

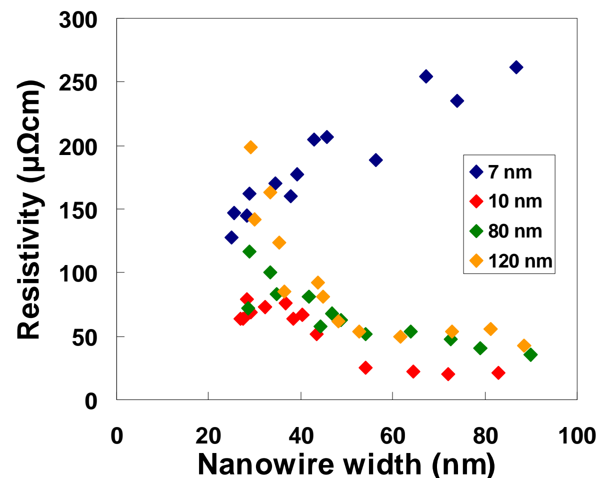

Fig.2: Dependence of Ni silicide resistivity on nanowire line width. Ni silicide formation was performed by the 2 step annealing process: 1st anneal at 270 °C for 2 min, unreacted Ni removal, and 2nd anneal at 500 °C for 1 min.

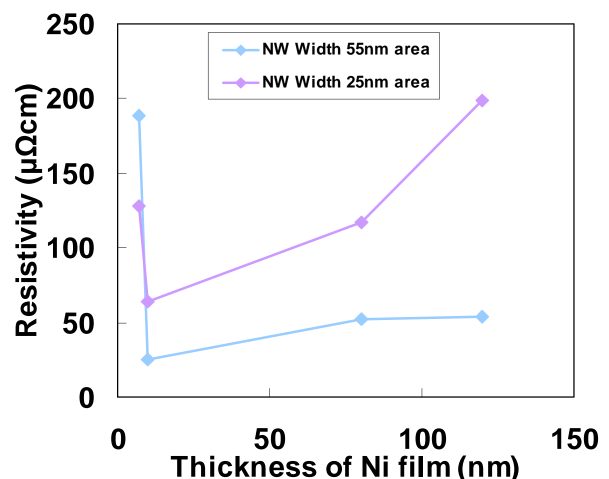

Fig.3: Dependence of Ni silicide resistivity on Ni film thickness. Nanowire widths were 55 nm and 25 nm.