

Group-IV Semiconductor Quantum Heterointegration by Low-Energy Plasma CVD Processing

Masao Sakuraba^{1,*} and Junichi Murota²

¹Laboratory for Nanoelectronics and Spintronics, Research Institute of Electrical Communication, Tohoku University

²Research Institute of Electrical Communication, Tohoku University

2-1-1 Katahira, Aoba-ku, Sendai 980-8577, Japan

*Tel: +81-22-217-5549, Fax: +81-22-217-6103,

E-mail: sakuraba.masao@myad.jp

1. Introduction

To create quantum-effect devices with Si-based group-IV semiconductors for heterointegration of new function on Si LSI, ultrathin film deposition with a few nanometer-order thickness and atomically controlled interfaces is important [1,2]. Plasma enhanced chemical vapor deposition (CVD) is expected to be an advanced epitaxial growth process to improve interface flatness and abruptness by lowering epitaxial growth temperature. In this paper, recent progress in (1) development of room-temperature resonant-tunneling diode using group-IV semiconductors and (2) low-energy plasma CVD processing for group-IV semiconductor quantum heterointegration are reviewed.

2. Development of room-temperature resonant-tunneling diode using group-IV semiconductors

By using low-temperature thermal CVD, atomically controlled formation of strained $\text{Si}_{1-x}\text{Ge}_x/\text{Si}(100)$ quantum heterostructures has been investigated and we can obtain improved negative differential conductance (NDC) characteristics of hole resonant tunneling diode (RTD) with nanometer-order thick strained $\text{Si}_{1-x}\text{Ge}_x$ layers and unstrained Si layers (Fig. 1) [1,2]. Here, especially to suppress the roughness generation at heterointerfaces for higher Ge fraction, Si barrier deposition using Si_2H_6 reaction at as low temperature as 400 °C is more effective compared to SiH_4 reaction at 500 °C after high-Ge-fraction strained $\text{Si}_{1-x}\text{Ge}_x$ growth. As a result, difference between peak and valley currents in NDC characteristics was effectively enhanced at 11 K to room temperature. Additionally, only about 1 nm-thick Si layer acts as barrier for resonant tunneling and heavy atomic-layer doping of impurity (e.g. C, N and so on) is expected to influence the barrier properties. Moreover, because further improvements in NDC is expected by suppression of thermal intermixing at the heterointerfaces, lower-temperature epitaxial growth process (e.g. low-energy plasma CVD) becomes increasingly important to modulate electronic properties of nanometer-order ultrathin layers of group-IV semiconductor far from thermal equilibrium. These are the motivation to develop low-energy plasma CVD processing.

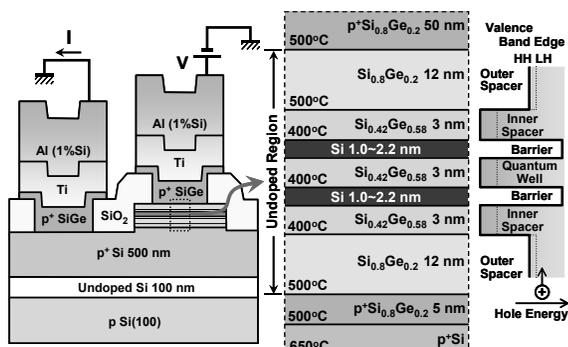


Fig. 1. Schematics of $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ hole resonant tunneling diode.

3. Low-energy plasma CVD processing for group-IV semiconductor quantum heterointegration

Atomically controlled surface reaction of reactant gases (SiH_4 , GeH_4 and B_2H_6) for deposition on $\text{Si}(100)$ can be enhanced under low-energy Ar plasma irradiation without substrate heating and this is effective to avoid plasma damage and intermixing (Fig. 2(a)) [3,4]. Formation of highly strained epitaxial heterostructures of Si and Ge has been also achieved in the range of a few nm thickness [4]. Moreover, control of Ge fraction at epitaxial growth of $\text{Si}_{1-x}\text{Ge}_x$ alloy films on $\text{Si}(100)$ has been also realized.

Additionally in order to introduce 2-dimensional lattice strain as well as high-concentration carriers and/or ionized impurity to modulate electronic properties, heavily doping in group IV semiconductors has been investigated. It has been confirmed that a Si cap layer can be epitaxially grown on high-density B adsorbed $\text{Si}(100)$ at an impurity atom amount as high as $7 \times 10^{14} \text{ cm}^{-2}$ and that most of the incorporated impurity atoms can be confined in a few nm-thick region (Fig. 2(b)) [5]. Especially for application to low-resistive electrode formation, epitaxial growth of in-situ heavily B-doped Si and Ge films on $\text{Si}(100)$ without substrate heating has been realized, although further improvements in electrical activation at low temperature are necessary.

In this way, low-energy plasma CVD processing are expected to be effectively applied to high-performance group-IV semiconductor heterodevices under suppression of dislocation generation and intermixing, i.e. group IV semiconductor quantum heterointegration on Si LSI.

Acknowledgments

This study was partially supported by a Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science and Technology of Japan and Japan Society for the Promotion of Science (JSPS) Core-to-Core Program "Atomically Controlled Processing for Ultralarge Scale Integration".

References

- [1] T. Seo, K. Takahashi, M. Sakuraba and J. Murota, Solid-State Electron. 53, (2009) 912.
- [2] K. Takahashi, M. Sakuraba and J. Murota, Solid-State Electron. 60 (2011) 112.
- [3] M. Sakuraba, D. Muto, M. Mori, K. Sugawara and J. Murota, Thin Solid Films 517 (2008) 10.
- [4] M. Sakuraba, K. Sugawara and J. Murota, Key Engineering Materials, 470 (2011) 98.
- [5] T. Nosaka, M. Sakuraba, B. Tillack and J. Murota, Thin Solid Films, 518 (2010) S140.

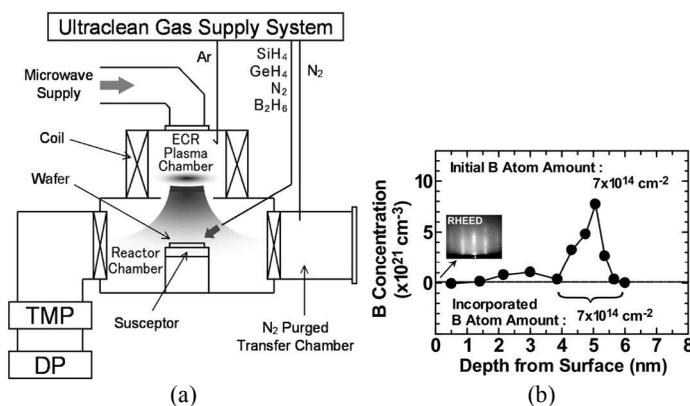


Fig. 2. (a) Schematic of ECR Ar plasma CVD system. (b) B concentration profile of heavily B atomic-layer doped Si (100) with a 5 nm-thick Si cap layer epitaxially grown on high-density B adsorbed $\text{Si}(100)$.