CVD/ALD-Mn(Nx) as Copper Diffusion Barrier for Advanced Interconnect Technologies

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In advanced integrated circuits,the interconnections between transistors are made of copper wires isolated by a low dielectric constant material in a damascene architecture. To prevent copper diffusion into the neighboring regions, commonly, a PVD-TaN/Ta liner is formed on the dielectric surface as a diffusion barrier prior to Cu metallization. As the wire width decreases when the technology node scales down, the barrier thickness must also be reduced in order to leave a maximum volume for the copper in the trench and thus to maintain the circuit performance. Because of the intrinsic limited step coverage of the PVD technique,it is very difficult to make a thin, conformal and continuous barrier. The integrity of the PVD-TaN/Ta barrier is expected to reach its limit at a trench dimension between 20nm and 30nm wide. As a result,alternatives must be found for further technology scaling. In recent years, Mn-based barriershave received great consideration as a thin self-formed MnSixOy diffusion barrier can be formed at the surface of the insulator without significant impact on the dielectric constant whilst preserving the whole trench volume for Cu filling[1)].Firstly, such a "zero-thickness barrier'' has been made using a PVD-CuMn seed layer, from which Mn atoms diffuse after a thermal anneal towards the surface of the insulator and form the diffusion barrier. However, because of the use of PVD, limited scalability of this option is expected. Therefore, CVD of Mnfrom $(EtCp)_2Mn$[2)]and bis(N,N0-diisopropyl-pentylamidinato) manganese (II)[1)]has been developed to enable the formation of a conformal barrier. In this work, we have investigated the barrier propertiesof different Mn-based layers by the so-called Time Dependent Dielectric Breakdown (TDDB) technique using a metal-insulator-semiconductor (MIS) planar capacitor (p-cap) structure[3)] (see figure1).In opposition to the damascene architecture,this unique design planar capacitorallows to assessthe intrinsic barrier propertiesin a copper/barrier/SiO_2system. Indeed, the TDDB is not affected by the integration factors such as Cu residues on the surface of the dielectric after Cu chemical mechanical polish (CMP) andthe line edge roughness (LER)). Figure 2shows the TDDB (E-model extrapolation) lifetimes of CVD-Mnlayers with thickness in the range of 1 to 2.3nm, which are comparable to the 6nm industry established PVD-TaN/Ta and much above 10 years specification.In this work, we also have investigated the Mn-nitridelayersas Cu diffusion barriersformed by either CVD or ALDmethods.Figure 3 and 4 show the TDDB performance of a Mn-nitride films with thickness in the range of 1to 2nm formed by CVD and ALD techniques, respectively. As can be clearly observed, MnNx layers also show similar barrier properties compared to a 6nm-PVD-TaN/Ta layer.

In conclusion, we have shown that Mn(Nx) in the range of 1 to 2nm deposited by CVD or ALD methods is an effective copper diffusion barrierwith performance comparable to a 6nm standard PVD-TaNTa barrier. This makes Mn(Nx)a serious candidate as copper diffusion barrier for advanced technology nodes.

The film properties, growth behavior and electrical performances obtained on damascene devices will also be reported and discussed in details.

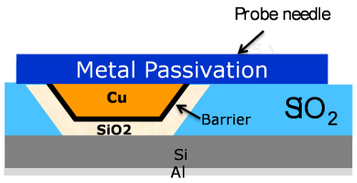

Figure1: Planar capacitor schematic used to evaluate the intrinsic barrier propertiesin a copper/barrier/SiO_2system.

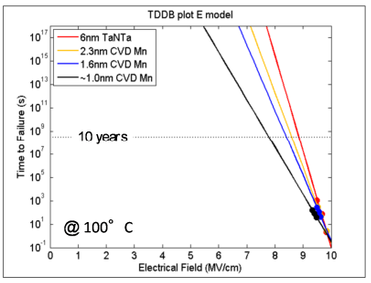

Figure2: TDDB lifetime of CVD-Mn of various thicknesses and 6nm PVD-TaNTa barrier on SiO_2.

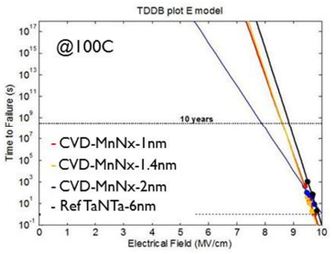

Figure 3: TDDB lifetime of CVD-MnNx of various thicknesses and 6nm PVD-TaNTa barrier on SiO_2.

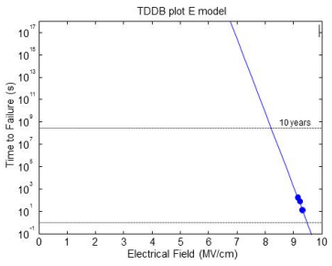

Figure 4: TDDB lifetime of 1nm ALD-MnNx barrier on SiO_2.

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