Non-Volatile Memory Technology: Directions Beyond Floating Gate Devices

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Since the first flash memory products arrived in the 1980's, they have both defined and dominated the markets for non-volatile semiconductor memory. While flash products have been developed to serve a broad range of applications, they all rely on the same basic device for data storage: the floating gate cell. Though this cell has shown a remarkable level of flexibility and scalability, two issues have driven significant investment in alternative technologies. First, the ability to reduce the cell dimensions below 20nm while maintaining the required performance and reliability has been challenging. Second, the standard floating gate cell might not have the capability to serve as a "storage class memory", a recently proposed addition to the computing memory hierarchy.

Beyond floating gate, a number of technologies are emerging to both provide a scaling path below 20nm and in some cases enable new types of system level memory architectures. Broad acceptance in either case has significant hurdles: the former requiring the ability to cost-compete with flash and the latter requiring system-level enablement. In addition, these technologies are typically based on new materials or physical mechanisms that have not been proven in mass production, and for both volume and cost reasons they must be compatible with existing manufacturing facilities. Several technologies have shown the potential to overcome these challenges, including PCM, RRAM, FERAM, and STT-RAM. This has driven significant investment across the industry and has enabled them to be demonstrated at maturity levels ranging from large-array test chips to low-volume commercial products.

This paper will first focus on the evolutionary path of floating gate-based devices, particularly NOR and NAND flash. This will include their current direction and limitations for meeting future memory requirements. It will then consider the potential and challenges of the leading emerging memory technologies to either supplant flash memory or enable their position in a new memory hierarchy.