Physical, Electrical, and Reliability characteristics of multi-Step Deposition-Annealed HfO_2 Film

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Introduction- The scaling down of the gate oxide thickness in metal-oxide-semiconductor (MOS) device to achieve high-speed operation and low-power consumption is continuous [1]. However, as the traditional thermal silicon dioxide (SiO_2) gate dielectric is scaled down to below 1.5 nm , a higher leakage current induced by direct tunneling become a serious issues and stop the proceeding of scaling roadmap [2]. To solve these problems, some alternative materials with a higher dielectric constant (high-*k*) have been studied to replace the conventional SiO_2 [3]. Among various high-*k* materials being studied, HfO_2 thin films have attracted great interest due to their potential applications as high-dielectric constant materials, large band gap, thermal stability and stable on silicon substrate [1,3]. The main purpose of this study is to compare the reliability of HfO2 high-k gate dielectric that are formed by a single-step deposition-annealing method with that of such a dielectric formed by a multi-step method. The effects of the static and dynamic stress on the reliability of multi-step deposition-annealed HfO_2 dielectric are systematically elucidated.

Experimental- After performing the standard RCA clean, the HfO_2 thin film were deposited on the *p*-type Si (100) wafers with a resistivity of 1-10 ohm-cm were deposited using atomic layer deposition (ALD) method. The precursors used for the HfO_2 film deposition were TEMAH ($Hf[NCH_3(C_2H_5)_2]_4$) and water (H_2O). The substrate temperature was kept constant at 200°C during the deposition. For a single-step deposition-annealing process, the deposition cycle is 80 cycles, which each cycle consists of H_2O and TEMAH purge times with 0.015 s and 0.25 s, respectively. After formation of the gate dielectrics, a thermal annealing was conducted at 750°C in N_2 gas for 30 s using rapid temperature process (RTP). In the case of multi-step deposition-annealing process, the deposited HfO_2 film was annealed at the same condition before completing 80 cycle deposition. In this study, two- and four-step deposition-annealing processes were employed. After completing deposition-annealing process, a 500 nm-thick aluminum (Al) layer was deposited on top of the thin HfO_2 films using evaporation methods. This layer was then patterned by lithography and etching processes to form the gate electrode. Finally, all devices received backside aluminum deposition and thermal annealing at 425°C. The fabricated devices used for electrical and reliability measurements had an electrode area of 7854 μm^2. The thickness of HfO_2 thin film was measured using Transmission electron microscopy (TEM). Capacitance-voltage (*C-V*) and current-voltage (*I-V*) measurements were done at room temperature using Keithley 590 analyzer and Keithley 238 high current source measure unit. In reliability measurement, the static stress (DC) is the conventional constant-voltage stress technology, and the dynamic stress includes the unipolar and the bipolar stresses.

Results and Discussion- Figure 1 presents the representative HRTEM images of the HfO_2 films with 80 deposition cycles for the deposition-annealing steps for: (a) as-deposited HfO_2/Si, (b) single-step annealed HfO_2/Si, (c) two-step annealed HfO_2/Si, and (d) four-step annealed HfO_2/Si. All HfO_2 films have two layers- the interfacial layer (IL) and the upper bulk HfO_2 layer. The thicknesses of the interfacial layer and the upper layer are presented in the HRTEM images. The thickness of the interfacial layer increases with the number of deposition-annealing steps. The four-step annealed sample had the largest interfacial layer thickness because the oxidation time at a high temperature (750°C) increased. Therefore, the interfacial layer grows continuously during repeated annealing. Additionally, annealing densified all upper HfO_2 layers and reduced the thickness to an extent that increased with the number of deposition-annealing steps. However, the extent of growth of the interfacial layer and densification of the upper HfO_2 layer decreases as the number of deposition-annealing steps increased. Additionally, the TEM image revealed that the as-deposited HfO_2 film remained amorphous and became polycrystalline structure upon annealing. Furthermore, multi-step deposition-annealing process yields a single-crystallized HfO_2 layer. Grazing incidence x-ray diffraction (XRD) analysis was performed to investigate the crystal structure of HfO_2 thin films as presented in Fig. 2. The as-deposited HfO_2 films were structurally amorphous and yielded no clear diffraction peak. The XRD spectra after post-deposition annealing reveals that HfO_2 films that are grown by single-step deposition-annealing process crystallize in a mixture of monoclinic and orthorhombic phases, while those grown by multi-step deposition-annealing process contains less of the crystallizes phases. A crystal nucleation event occurs at any point during the ALD process, and probable sites for such events are defect or impurities. Additionally, crystallite growth generally proceeds both laterally and vertically, but tends to favor the vertical direction. Therefore, a long deposition time enables increased crystallite nucleation and growth [3,4]. However, these defect or impurity nucleation points can be eliminated by high-temperature annealing before growth.

C-V characteristics of the Al/HfO_2/*p*-Si (MOS) devices that had undergone different HfO_2 deposition-annealing processes were compared. These *C-V* curves reveal that the HfO_2 film that underwent more deposition-annealing step had a higher capacitance in accumulation, and therefore a lower EOT value. However, the accumulation capacitance of the HfO_2 capacitor that underwent single-step deposition-annealing is lower than those of the non-annealed, yielding a higher EOT value due to a thicker interfacial layer. Additionally, Table I summarizes the electrical results that are extracted from the *C-V* curves as well as the physical thickness of each layer in the HfO_2 capacitors that had undergone various deposition-annealing steps.

The time-dependent-dielectric-breakdown (TDDB) of the HfO_2 devices was evaluated at three voltages under static stress. The time to breakdown was determined using the time when the gate current density abruptly increased. Figure 3 compares the dielectric breakdown failure time at a failure rate of 63.2 % as a function of the stressing electrical field among HfO_2 capacitors that had undergone various number of deposition-annealing steps. As presented in the figure, the curves of the failure times versus the stressing electrical field of all HfO_2 capacitors that had undergone various numbers of deposition-annealing steps were almost parallel, indicating that their dielectric failure mechanisms were similar. Additionally, in a fixed electrical field, the order of the breakdown failure times was: four-step annealed > two-step annealed > non-annealed > single-step annealed samples. It was reported that the dielectric degradation is a composite effect of charge trapping in the oxide and at the interface and the creation of neutral trap under stress. As the total number of traps reached the critical value for establishing a conducting path between the electrodes, dielectric breakdown occurred [5]. The breakdown times of the HfO_2 devices that had undergone various numbers of deposition-annealing steps under unipolar and bipolar stresses were also compared. The failure times at a failure rate of 63.2 % were also obtained from the Weibull distributions. Table II compares experimentally determined static and dynamic stresses. All HfO_2 devices had a longer lifetime and a larger Weibull distribution under dynamic stress than under static stress. Additionally, bipolar stress yielded the longest dielectric breakdown time possibly because of a charge de-trapping mechanism within the dielectric that affects the defect density. With respect of the effect of the multi-step deposition-annealing, the four-step deposition-annealed HfO_2 device had the longest dielectric breakdown time under dynamic stress, but the magnitude of improvement seems to fall as the number of deposition-annealing steps increases. To compare the charge de-trapping effects among various multi-step deposition-annealed HfO_2 devices, Fig. 4 compares the lifetime enhancements (t_{63}(AC)/t_{63}(DC)) of the HfO_2 devices. The data demonstrate that the highest improvement in lifetime was that of the single-step deposition-annealed HfO_2 devices under bipolar stress, indicating that the de-trapping effect becomes more effective. The effective de-trapping effect can is attributable to more charge trapping in the single-step deposition-annealed HfO_2 devices.

Conclusions- This study compares the physical, electrical and reliability characteristics of the multiple-step deposition-annealed HfO_2 gate stack in detail. After 750°C high temperature annealing, the single-step HfO_2 has transformed into a polycrystalline phase, while the multi-step HfO_2 is found to remain in a nanocrystalline phase, indicating that a multi-step deposition-annealing method could significantly improve the thermal stability of the high-k HfO_2 film with respect to the grain formation process. These changes lead to an improvement in the electrical characteristics, breakdown voltage, and reliability of the multi-step HfO_2 film. Under dynamic stress, although single-step deposition-annealed HfO_2 film has a larger improvement in dielectric breakdown time due to more de-trapping effect, multi-step deposition-annealed HfO_2 films still exhibit a longer breakdown time. Therefore, the multi-step deposition-annealing method is a promising means for improving the thermal stability and reliability of high-k gate stacks.

References

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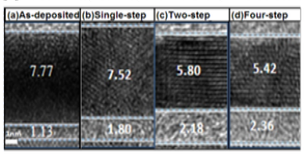

Figure 1: HRTEM images of (a) As-deposited (b) Single-step annealed (c) Two-step annealed (d) Four-step annealed.

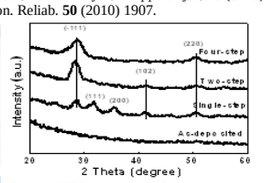

Figure 2: XRD spectra of HfO_2 film with various deposition-annealing steps.

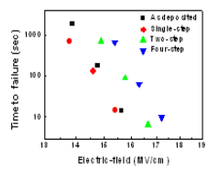

Figure 3: Dielectric breakdown time at 63 % failure rate for HfO_2 film with various deposition-annealing steps as functions of stress voltages.

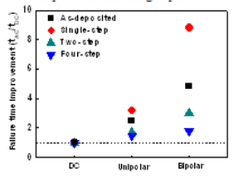

Figure 4: Lifetime enhancement of AC stressing for HfO_2 films with various deposition-annealing steps.

Table I: Summary of the electrical results and each layer thickness variations for HfO_2 films with various deposition-annealing steps.

Number of step	Total HfO_2 thickness by HRTEM (nm)	Thickness of interfacial layer (nm)	Thickness of bulk HfO_2 layer (nm)	Capacitance ($\times 10^{-14}$ F)	Dielectric constant of total HfO_2 film	Dielectric constant of bulk HfO_2 layer	EOT (nm)	Flatband voltage (V)	Hysteresis (V)
As-deposited	9.29 ± 0.16	1.52 ± 0.04	7.66 ± 0.12	6.77 ± 0.16	8.56	12.93	3.44	-0.95 ± 0.02	2.05 ± 0.05
Single-step	9.22 ± 0.31	1.80 ± 0.05	7.52 ± 0.26	6.25 ± 0.25	8.25	15.19	3.73	-0.84 ± 0.04	1.21 ± 0.06
Two-step	7.98 ± 0.32	2.18 ± 0.04	5.80 ± 0.28	6.97 ± 0.1	8.04	19.5	3.34	-0.72 ± 0.01	0.12 ± 0.01
Four-step	7.78 ± 0.27	2.36 ± 0.11	5.42 ± 0.16	7.12 ± 0.1	7.86	23.14	3.27	-0.75 ± 0.02	0.07 ± 0.02

Table II: The characteristic times (t_{63}) and Weibull slopes (β) for HfO_2 films d with various deposition-annealing steps under various stress conditions.

Number of step	Type of stress	t_{63} (s)	β
As-deposited	DC	22.1	1.34
	Unipolar	55.25	1.53
	Bipolar	106.743	2.55
Single-step	DC	13.5	1.26
	Unipolar	43.335	1.46
	Bipolar	118.935	2.62
Two-step	DC	147.9	1.61
	Unipolar	254.388	1.93
	Bipolar	449.616	2.88
Four-step	DC	488.5	1.83
	Unipolar	732.75	2.03
	Bipolar	884.185	3.24