Fabrication of Metal-Nitride/Si Contacts with Low Electron Barrier Height Keisuke Yamamoto<sup>1\*</sup>, Kojiro Asakawa<sup>2</sup>, Dong Wang<sup>2</sup>, and Hiroshi Nakashima<sup>1</sup> <sup>1</sup>Art, Science and Technology Center for Cooperative Research, Kyushu University <sup>2</sup>Interdisiplinary Graduate School of Engineering Sciences, Kyushu University 6-1 Kasuga-koen, Kasuga, Fukuoka 816-8580, Japan \*E-mail: yamamoto.keisuke@astec.kyushu-u.ac.jp

Fabrication of metal/semiconductor contact with low electron barrier height and low parasitic resistance is important for high-performance CMOS devices. Recently, we succeeded in the formation of a TiN/Ge contact with extremely low electron barrier height ( $\Phi_{BN}$ ) less than 0.1 eV, which was fabricated by direct sputter deposition from a TiN target and low temperature anneal at 350°C [1,2]. In this study, we apply this technique to Si to form low  $\Phi_{BN}$  contact.

The substrates were p- and n-type (100) Si with a resistivity of 10  $\Omega$ ·cm. A 50 nm-TiN film and 50 nm-Al film were deposited on the Si substrate by rf magnetron sputtering using a TiN target and thermal evaporation, respectively. The Al/TiN film was patterned using a lift-off technique. Finally, postmetallization annealing (PMA) was carried out at 400°C in N<sub>2</sub> for 10 min, which was the optimal PMA condition.

Figures 1(a) and 1(b) show the J-V characteristics for the TiN/p-Si and TiN/n-Si contacts, respectively. The TiN/p-Si contact showed rectifying behavior and TiN/n-Si contact showed Ohmic-like behavior. These J-V results suggest that the TiN/Si contact has high hole barrier height ( $\Phi_{BP}$ ) and low  $\Phi_{BN}$ . Actually, the  $\Phi_{BP}$  obtained from the forward J-V characteristic of TiN/p-Si was 0.85 eV. Note that the  $\Phi_{BP}$  found in this study is one of the highest barrier heights among metal/p-Si contacts, which is comparable to that of an ErSi/Si contact [3]. The  $\Phi_{BN}$  is obtained as 0.27 eV from the relation of  $\Phi_{BN} + \Phi_{BP} = E_g$ , where  $E_g$  is the energy bandgap of Si (1.12 eV).

For comparison, we also fabricated Ti/Si contacts using the same fabrication method. The J-V characteristics are also shown in Figs. 1(a) and 1(b). The  $\Phi_{BP}$  and  $\Phi_{BN}$  were obtained as 0.61 eV and 0.55 eV, respectively. These are in good agreement with the reported values of Ti/Si contact [4]. It is very interesting that the electrical characteristics drastically changed by the addition of N<sub>2</sub> gas during Ti sputter deposition, which is also represented in Figs. 1(a) and 1(b); with increasing an N<sub>2</sub> flow rate, J at reverse bias decreased on p-Si and increased on n-Si, moving towards the J-V characteristics of TiN/Si contacts. We will present the results for other binary metal nitrides.

We fabricated inversion-mode back-gate MOSFET with TiN metal S/D on p-type SIMOX-SOI substrate. The device structure is shown in the inset of Fig. 2. Figure 2 shows I<sub>D</sub>-V<sub>G</sub> characteristic for the back-gate MOSFET, indicating that channel conductions are well controlled by the V<sub>G</sub>. Thus, the back-gate MOSFET exhibits well-behaved n-type inversion-mode operation. The peak field effect mobility ( $\mu_{FE}$ ) estimated from the I<sub>D</sub>-V<sub>G</sub> characteristic was 650 cm<sup>2</sup>/Vs. The D<sub>it</sub> of the SOI/BOX interface estimated from the subthreshold slope of 203 mV/dec was  $1.1 \times 10^{11}$  cm<sup>-2</sup>eV<sup>-1</sup>. These values are comparable with universal electron mobility and D<sub>it</sub> value of SiO<sub>2</sub>/Si [5]. Thus, the test device structure with TiN S/D, which could be easily prepared without high

temperature process, is useful for the electrical characterization of SOI substrate.



Fig. 1 J-V characteristics of (a) TiN and Ti contacts on n-Si and (b) TiN and Ti contacts on p-Si. Measurement temperature for all samples is RT.



Fig. 2  $I_D$ -V<sub>G</sub> characteristic for the fabricated inversionmode back-gate MOSFET. The cross-sectional schematic image of the MOSFET is also shown as an inset.

References

- [1] M. Iyota et al., Appl. Phys. Lett. 98 (2011) 192108.
- [2] K. Yamamoto et al., Jpn. J. Appl. Phys. 51 (2012) 070208.
- [3] N. Reckinger et al., Appl. Phys. Lett. 94 (2009) 191913.
- [4] H. R. Liauh et al., Appl. Phys. Lett. 61 (1992) 2167.
- [5] H. Nakashima et al., Jpn. J. Appl. Phys. 43 (2004) 2402.