# Development of Metal Source/Drain Ge-CMOS using TiN/Ge and HfGe/Ge contacts

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Ge is of great interest as a candidate channel material for future CMOS devices due to its high intrinsic carrier mobility. To translate this potential into CMOS devices, there are several technical problems, which are formations of a high-quality gate-stack and source/drain (S/D) junction, and barrier height ($\Phi_B$) control for a metal/Ge contact. Among them, the $\Phi_B$ control of a metal/Ge contact is very difficult because the Fermi level is strongly pinned near the valence band edge at any metal/Ge interfaces [1]. Thus, in order to embody Ge-CMOS with metal S/D structures, a metal/Ge contact with low electron barrier height should be developed.

Recently, we succeeded in Ohmic contact formation on a moderately n-doped Ge by direct sputter deposition from a TiN target and subsequent postmetallization annealing (PMA) at 350°C. The electron barrier height ($\Phi_{BN}$) and hole barrier height ($\Phi_{BP}$) were 0.18 eV and 0.50 eV, respectively [2]. By optimizing the TiN deposition condition, we succeeded in a further decrease in $\Phi_{BN}$ less than 0.10 eV [3].

In this paper, first, we show the fabrication and the electrical properties for TiN/Ge contacts. Second, we show the fabrication and the electrical properties of the HfGe/Ge contacts with low $\Phi_{BP}$. Third, we present device performances of metal S/D n- and p-MOSFETs using TiN and HfGe as S/D, respectively. The device operations will give us a realistic candidate for next-generation CMOS.

## 1) Contact fabrications and the electrical properties

After chemical cleaning and photoresist patterning, a TiN film was directly deposited on (100) Ge substrate by rf magnetron sputtering using a TiN target with a Ti:N ratio of 1:1. Then, a 50-nm-thick Al film was deposited by thermal evaporation, and the Al/TiN contact pattern was formed by the removal of photoresist. Finally, postmetallization annealing (PMA) was carried out at 350°C in $N_2$ for 10 min.

The *J-V* characteristics of TiN/p-Ge and TiN/n-Ge contacts showed rectifying and Ohmic features at room temperature, respectively. The $\Phi_{BP}$ was obtained as 0.53 eV. However, the *J-V* characteristics TiN/p-Ge and TiN/n-Ge contacts changed to Ohmic and rectifying features after PMA at 600°C, respectively.

We also investigated STEM images for TiN/Ge contacts after annealing at 350 and 600°C. An amorphous interlayer (IL) with a thickness of 2 nm, which consists of Ti and Ge, was observed in STEM image of TiN/Ge contact prepared at 350°C. On the other hand, the amorphous IL disappeared after annealing at 600°C, and TiN was directly contacted with Ge crystal, leading to Ohmic feature of TiN/p-Ge contact. Thus, it was concluded that the amorphous IL alleviates the Fermi level pinning.

From circular transmission line measurement, the contact resistivity of TiN/$n^+$-Ge contact was estimated as $7.9\times10^{-6}$ Ω·cm$^2$ (P surface concentration: $4\times10^{19}$ cm$^{-3}$), which suggests that the IL is conductive. From our recent study [3], it was found that the TiN/p-Ge contact with $GeO_2$ passivation shows $\Phi_{BP}$=0.57 eV, corresponding to $\Phi_{BN}$=0.09 eV.

We also found that HfGe is useful for low $\Phi_{BP}$ contact, which was fabricated by sputtering using Hf target. From the *J-V* characteristic of HfGe/n-Ge contact, the $\Phi_{BN}$=0.60 eV was obtained. The HfGe/p-Ge contact showed an Ohmic behavior even at 100 K. Thus, we founded that TiN and HfGe are useful for metal S/D n- and p-MOSFETs, as shown in Fig. 1.

## 2) Performances of metal S/D MOSFETs

We fabricated metal S/D p- and n-MOSFETs using HfGe and TiN as S/D, respectively. The detail process flows have been described elsewhere [4]. Here, we used the same gate last process except for gate Al-PMA, which is useful for p-MOSFET but harmful for n-MOSFET [5]. Thus, the PMAs were performed at 400 and 300°C for p- and n-MOSFETs, respectively.

The output and transfer characteristics of both MOSFETs showed well-behaved transistor operations. The field effect carrier mobilities were evaluated from the transfer characteristics. The peak hole mobility ($\mu_h$) was 336 cm$^2$/Vs, which is almost the same as previous result (370 cm$^2$/Vs) from p-MOSFET with $p^+$ S/D [5]. This high $\mu_h$ should come from a thick HfGe layer with a thickness of approximately 10 nm and an effective Al-PMA. By contrast, the peak electron mobility ($\mu_e$) was 223 cm$^2$/Vs, which is much lower than that (790 cm$^2$/Vs) from n-MOSFET with $n^+$ S/D [5]. This low $\mu_e$ would come from a poor interface properties of a gate stack because the gate stack should be fabricated at a maximum temperature of 400°C. Thus, low temperature fabrication for high-quality gate stack must be established for an increase in $\mu_e$.

We found that $\Phi_{BP}$ of TiN/Ge and $\Phi_{BN}$ of HfGe/Ge are 0.53 and 0.60 eV, respectively, which are available to metal S/D in n- and p-MOSFETs. We fabricated the MOSFETs and demonstrated the devices operation. The MOSFETs worked successfully, which open a method for embodying the metal S/D Ge-CMOS.

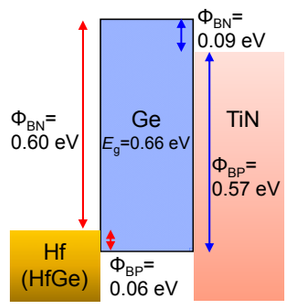


**Fig. 1** Band diagram of HfGe/Ge and TiN/Ge contacts. The HfGe/Ge and TiN/Ge are preferable as low barrier height contacts for hole and electron, respectively.

## References

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