The Effects of Defects on the Breakdown Voltage of GaN High Power Electronic Devices K.A. Jones¹, M.A. Derenge¹, R.P. Tompkins¹, K.W. Kirchner¹, J. Leach², P. Suvarna³, and F. Shahedipour³ ¹Army Research Lab, Adelphi, MD 20783 ²Kyma Technologies, Raleigh, NC 27617 ³CNSE, SUNY-Albany, Albany, NY 12203

GaN high power electronic (HPE) devices theoretically have the potential to operate more efficiently than equivalent SiC devices because GaN has a larger critical electric field, F_C , and bulk electron mobility, μ_B . In addition, the electron mobility, μ_C , in the 2-dimensional electron gas (2DEG) created at the AlGaN/GaN interface of the high electron mobility transistor (HEMT) can be twice as large, whereas μ_C in a SiC MOSFET is often 20 times smaller than μ_B . The carrier concentration in the channel, n_C , is also usually larger in the HEMT because there is a positive polarization charge at the interface so the current carrying capability of the HEMT is larger.

However, GaN HPE devices have fallen far short of their potential because the material is so defective. One reason could be that it contains a large number of crystalline defects, primarily dislocations, $(\sim 10^9 \text{ cm}^{-2})$ when the device structures are grown on hetero-substrates such as SiC or Si, which have a relatively large lattice mismatch with GaN. The focus of the theoretical calculations is on how threading edge dislocations that are negatively charged scatter the electrons thereby reducing their mobility¹, but little is said about how they affect the breakdown voltage, V_B. There is evidence that, although their concentration is significantly less than those of the threading edge or mixed dislocations, threading screws have a more profound effect, as is demonstrated in how much they increase the gate leakage current². It has been suggested that they are able to do this because their core contains Ga-Ga and N-N bonds as well as the strained Ga-N bonds that create states in the energy gap through which carriers can hop³. This leads to the soft premature breakdown often seen in GaN HPE devices. This explanation is given credence by the sharp, large V_B recently observed by Kizilyalli *et al.*⁴ that they attribute to avalanche breakdown. They attribute their success to having high quality material in addition to properly designed field plates.

The well known equation for the minimum specific onresistance, R_{ON} , for a diode for which it is assumed that none of the voltage drop is across the junction, the film thickness is equal to the depletion layer width at breakdown, and all of the electron concentration is equal to the net dopant concentration is,

$$R_{ON} = 4V_B^2 / (\varepsilon \mu_B F_C^3)$$

where ε is the electric permittivity. This equation often appears as a log-log plot with points for experimental data showing how close one has come to the theoretically best value. The ratio of the magnitude of the denominator for the material of interest to that for silicon is often called the Baliga figure of merit (BFOM). This equation can also be reconstructed to determine the maximum V_B for a given net doping concentration in the diode drift region, n_D, which is,

$$V_B = \varepsilon F_C^2 / (2qn_D)$$

where q is the charge on an electron.

People in the past have not been too concerned about the relatively large concentration of unintentional dopants

(UID) because their effects were dominated by those of the large number of dislocations. The usual n-type UIDs are Si and O, and their concentrations as determined by secondary ion mass spectroscopy (SIMS) are almost always in the low to mid 10^{16} cm⁻³. This seems to be true for films grown by metal-organic chemical vapor deposition (MOCVD) or hydride vapor phase epitaxy (HVPE). The source of oxygen has been attributed to H_20 in the NH₃. If true this could be a problem because of the relatively large V/III ratios used during growth - 500 · 2500 for MOCVD and 20 - 200 for HVPE. It has not yet been shown that HVPE material contains less O than MOCVD films so this might not be the case, but it could also be due to the fact that O is added to the gas stream when HCl in the HVPE system reacts with the quartz tube. Historically, people were concerned about not being able to grow AlGaAs films because of the strong tendency for Al to getter O from the H₂O in the AsH₃ gas stream, but the problem was solved by improving the purity of the AsH₃. Perhaps the UID O concentration can be reduced by improving the purity of the NH₃. At one time it was thought that HVPE GaAs would always contain a larger UID concentration because of the reactions of the unreacted HCl with the quartz growth tube, but it was shown that neither Si nor O was a primary contaminant⁵ down to the low 10¹⁴ cm⁻³, suggesting that problems with reactions with the growth chamber have been over estimated even though GaN is grown at temperatures 300 - 400°C higher. The primary acceptor in MOCVD GaN is C⁶, and even when the films are grown at higher pressures, its concentration is in the mid 10^{16} cm⁻³ range⁷. We determined that in some cases its concentration exceeded the sum of the Si and O concentration as determined by SIMS⁸, but the sample was still n-type suggesting that either the difference was made up by N vacancies, which are believed to be donors, or that not all of the C occupied acceptor sights. The C acceptor in the n-type material contributes to premature breakdown either by being emptied by the field in the depletion layer or by being more easily ionized.

We have developed an annealing cap that enables us to anneal GaN wafers at temperatures as high as 1300°C for times as long as 30 min without significant damage to the GaN surface. It is clear that there is atomic movement, as the surface roughens and both symmetric and asymmetric rocking curve widths decrease indicating that the dislocation concentrations were reduced. These changes and changes in the electrical and optical properties caused by the anneal will be used to highlight the importance of using purer material with fewer structural defects.

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GaN devices have great potential for high power electronic applications, but they have not yet realized their potential primarily because the material contains a large concentration of dislocations and unintentional dopants. Their detrimental effects and sources of origin are reviewed, and methods for their reduction are discussed. It will be shown that the concentration of dislocations can be reduced significantly and the point defect concentrations can be altered using an annealing cap we have developed that enables us to anneal GaN wafers at temperatures as high as 1300°C for times as long as 30 minutes without N evaporating preferentially when the surface of the films when they are smooth. We will show that the dislocation concentrations can be reduced and the electrical and optical properties can be altered. These processes will be discussed and we will describe how they can be used to improve the properties of the devices.

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