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Progress in the Resolution of Materials Challenges for High-Voltage SiC Power Devices

D.K. Gaskill[1], R.L. Myers-Ward[1], Z.R. Robinson[1], V.D. Wheeler[1], P.B. Klein[1], N.A. Mahadik[1], R.E. Stahlbush[1], L.O. Nyakiti[1], A. Nath[2], and C.R. Eddy, Jr.[1]

[1]U.S. Naval Research Laboratory, 4555 Overlook Ave., SW, Washington, DC 20375
[2]George Mason University, Fairfax, VA 22030

Silicon carbide (SiC) is a material of interest for high-temperature, high-voltage and high-power switching device applications. Key materials challenges inhibiting such devices include elimination of basal plane dislocations (BPDs) and enhancement of minority carrier lifetimes in the drift or blocking regions of the device. Recent progress in addressing both of these issues is presented.

BPDs are a major concern for the SiC bipolar devices required for high-voltage applications as they source Shockley-type stacking faults in the presence of an electron-hole plasma and reduce minority carrier lifetimes. Many methods have been investigated to reduce the BPD density including pre-growth treatments, substrate orientation, growth parameters and growth interrupts. It has been shown that the conversion of BPDs to threading edge dislocations (TEDs) continues throughout the epitaxial growth process in 4° off-axis SiC material and that a minimum thickness of ~16 µm is required to convert all BPDs to TEDs. Here we show that optimizing a hydrogen etch of the substrate prior to epitaxial growth significantly enhances conversion efficiency in a thin (~6.5 µm), highly doped n$^+$ buffer layer (BL).

Epitaxial layers were grown on 4° off-axis substrates in an Aixtron/Epigress VP508 horizontal hot-wall reactor using the standard chemistry of silane (2% in H_2) and propane. Prior to growth, the substrate was hydrogen etched for various times (50 and 90 min), temperatures (1620, 1650, and 1665 °C) and pressures (40, 70, 100 and 130 mbar). After the H_2 etch procedure, the process conditions were adjusted to the growth conditions which were fixed at T = 1620 °C, P = 100 mbar and C/Si = 1.55. An initial ~6 µm thick highly doped (~ 9x10^{17} cm^{-3}) n$^+$ BL was grown using ultra high purity nitrogen as the n-type dopant, followed by an unintentionally doped (UID, $N_A - N_D < 2.5\times10^{14}$ cm^{-3}) film of 8 - 20 µm to permit characterization of the BPDs. Before growth, the substrates structural quality was investigated using X-ray rocking curve maps. Ultraviolet photoluminescence (UVPL) imaging was used to identify the BPDs after epitaxial growth. The surface roughness was analyzed using atomic force microscopy, while the large area morphology was evaluated using Nomarski microscopy and Zygo optical profilometry.

Etch temperature and pressure was found to have the largest influence on BPD conversion compared to etch time. The density of BPDs was slightly reduced in an epilayer without a buffer layer from ~50 cm^{-2} to ~40 cm^{-2} when employing a 50 min H_2 etch prior to growth compared to that of a standard 5 min etch at a temperature of 1620 °C. However, when the etch temperature was raised to 1650 °C and a ~6.5 µm BL was included, the BPD density at the BL/UID interface was drastically reduced to ~ 2 cm^{-2}; the average density for a sample with a 5 min H_2 etch at 1620 °C prior to growth and a 5 µm BL is ~ 18 cm^{-2}. When the temperature was raised further to 1665 °C, no significant enhancement was observed. Reduced etch pressures were also investigated for a substrate originating from a different boule with a fixed etch temperature of 1665 °C and time of 90 min. As seen in Fig 1, the density of BPDs after a 6 µm buffer layer decreased as the pressure increased, until it reached a minimum, whereby further increase in pressure increased the BPD density. The highest conversion occurred at a pressure of 70 mbar during the H_2 etch prior to growth, which resulted in a density of ~6 BPD cm^{-2}.

In an effort to understand the fundamental processes involved in chemical vapor deposition of SiC, low energy electron microscopy (LEEM) was used. This technique allowed for *in situ* observation of SiC island nucleation, growth and island coarsening. By monitoring island shape and size a function of time, the rate limiting process in SiC growth can be determined. A detailed study has been initiated, including computer simulations of experimental data, and new results will be presented.

Additionally, efforts to improve minority carrier lifetime in epi-layers has focused solely on growth approaches to date. Using various growth approaches, low-doped epitaxial layers of only 20 µm in thickness on a 5 µm highly doped buffer layer have demonstrated minority carrier lifetimes up to 4 µs, as measured by time resolved photoluminescence, without any pre- or post-processing treatment.

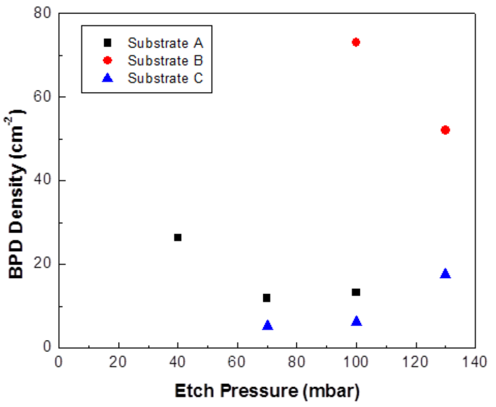

Figure 1. BPD density as a function of etch pressure for a constant etch time of 90 min and an etch temperature of 1665 °C.

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