Key Reliability Issues for SiC Power MOSFETs

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Even with the successful introduction of SiC power MOSFETs into the commercial market place, several key reliability issues have not been fully resolved. The main two issues are the stability of the device threshold voltage, V_T, and the reliability of the gate oxide.

An excess negative shift of V_T under high-temperature reverse-bias (HTRB) conditions can lead to a critical increase in *OFF*-state leakage current and potential device failure (see Fig. 1) [1]. Although a number of different types of interfacial charge are present either in the insulating gate oxide or at its interface with the SiC conduction channel, the primary defects are near-interfacial oxide traps [2, 3].

Both research and commercial-grade devices exhibit a gate bias-induced V_T instability effect, wherein a positive-bias stress shifts V_T positively, and a negative-bias stress shifts V_T negatively. This effect is repeatable, and caused by the direct tunneling of electrons either into or out of these near-interfacial oxide traps, depending on the applied gate bias. These effects are exaggerated for longer bias-stress times or greater oxide electric fields. Not surprisingly, the magnitude of this V_T instability is affected by the device processing, in particular whether a nitrogen-based post-oxidation anneal was performed [2].

The measurement conditions following the gate-bias stress have a strong effect on the degree of V_T instability observed. For example, a much smaller V_T shift is seen when V_{GS} is swept positively in the conventional manner, from accumulation to inversion for n-channel devices, following a positive-bias stress than if V_{GS} is swept negatively. Likewise, much smaller V_T instabilities are observed if V_{GS} is swept slowly than for faster measurements (a 100-µs gate sweep typically shows a four times larger effect than a more conventional 1 to 10-s measurement) [2]. The reason for this is the acute sensitivity of the charge state of near-interfacial oxide traps to the applied gate bias during the measurement. The more different the measurement bias, and the longer it is applied, the more it counteracts the effect of the previously applied stress bias. A two-way tunneling model has been successfully developed that accounts for the dependence of the V_T instability on both the stress and measurement times by allowing for the simultaneous tunneling in and out of electrons, wherein a steady-state balance occurs in the wake of the tunneling front [4].

Similar V_T instabilities are observed in both lateral test structures and fully-processed vertical power devices [3]. Similar instabilities are also observed in both 4H and 6H poly-types, in both MOSFETs and MOS capacitors, and in devices with either a thermal or deposited gate oxide. Effects due to self-heating when performing *ON*-state stress and allowing the rated current to flow through the device are very similar to those when externally heating the device during a gate-bias stress. Much larger V_T instabilities are observed in either case, compared with room-temperature gate-bias stressing. This is very likely due to the activation of additional oxide traps, which can then participate in the oxide trap charging process [3]. It is likely that interface traps are being generated as well, but this is not the cause of the increased V_T instability since the same interface trap charge state should exist when measuring the threshold voltage. Additional difficulties in sorting out the bias-temperature response may be due to the presence of mobile ions in some sample sets [5].

The gate oxides of SiC MOSFETs are similarly sensitive to ionizing radiation as are Si MOSFETs for oxides of a similar thickness. The radiation response may provide valuable insight into the bias-temperature response, since both effects are likely due to the activation of so-called E-prime centers in the oxide, which are related to an oxygen vacancy [1].

Existing reliability test standards (based on Si technology) have been demonstrated to be inadequate for SiC given that the same device may be deemed to have both passed and failed, simply as a consequence of the delay in the measurement that is allowed under present standards [6]. We have also shown that three different conclusions may be drawn as to the effect of bias temperature stress, depending on whether immediate high-temperature measurements, immediate room-temperature measurements (enabled by rapid cooling), or later room-temperature measurements are performed [7]. This is in addition to the effects of measurement speed and direction mentioned above.

In conclusion, although significant improvements in V_T stability have been demonstrated in state-of-the-art devices, the issue has not yet been full resolved. The full paper will also discuss issues related to extrinsic defects and gate-oxide reliability.

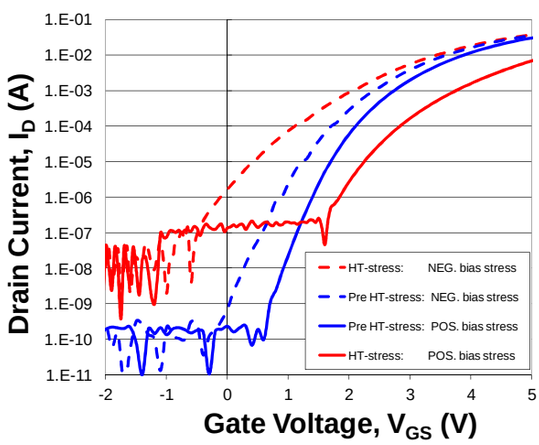

Figure 1. Potential reliability failure mode: negative threshold-voltage shift leading to increased leakage current under high-temperature reverse-bias stress condition.

References

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