On-axis 4H SiC Epitaxial Layers for High Power Applications

J.P. Bergman[a], J. Hassan[a], L. Lilja[a], A. Salemi[b], A. Hallen[b] and E. Janzén[a]
Email: peber@ifm.liu.se
[a]Department of Physics, Chemistry and Biology, Linköping University,
SE-581 83 Linköping, Sweden
[b]Lab of Materials and Semiconductor Physics, Royal Institute of Technology
P.O. Box Electrum 229, SE-16440 Kista, Sweden

4H-SiC high power bipolar devices have long been hindered due to high density of structural defects in the epilayers, mainly replicated from the off-cut substrate, and low minority carrier lifetime. On-axis homoepitaxial growth opens up a new route to realize the capability of 4H-SiC in the field of high power applications. This is mainly due to the fact that critical defects like basal plane dislocations (BPDs) which influence the bipolar device characteristics and other epitaxial defects can be completely avoided using on-axis growth. One obstacle with on-axis growth is the difficulty to maintain polytype stability, and a high density of 3C-inclusions or a complete 3C coverage are frequently observed.

We demonstrate on-axis homoepitaxial growth of 4H-SiC(0001) PiN structure on 3-inch wafers with 100% 4H polytype. Successful homoepitaxial growth was made after a careful in-situ surface preparation in a mixture of 0.006% SiH_4 in H_2 in a horizontal hot-wall CVD reactor equipped with SiC coated susceptor. Epilayers were grown at a growth rate of 7 µm/h, using standard gas phase chemistry (H_2+Ar+SiH_4+C_3H_8), C/Si ratio 1 and, at a temperature and pressure of 1600 ℃ and 100 mbar, respectively.

The layers were grown with a thickness of 105 µm, controlled n-type doping of $4x10^{14}$ cm^{-3} and, completely free of BPDs and in-grown stacking faults, as required for high power bipolar devices. The epitaxial layers has been C-implanted for lifetime enhancement and processed to high voltage PiN-diodes.

One of the major issues in on-axis epilayers is large inhomogeneity in the surface morphology, mainly due to different growth mechanisms iin different regions. Columnar shaped spiral growth occurs at threading screw dislocations, while step-flow growth occurs in regions with large local off-cut angle. Spiral growth is dominant in the regions where local off-cut is less than 0.1° and for large off-cut angles, step-flow g rowth is dominant. This gives a very rough surface with variations of several µm. For device processing this is not acceptable and a re-polishing step using CMP has been introduced after the growth of the thick drift layer to prepare the surface before growth of the p+/p++ anode layer.

The carrier lifetime is an important parameter for high voltage bipolar devices, and we have observed a difference in lifetime between regions grown with spiral as compared to step-flow growth. A higher lifetime is observed in the spiral growth regions. This difference was also present after the C-implantation (at 600 ℃) and an nealing step (1550 ℃ for 1 hour and slow cooling down), which increased the optically measured carrier lifetime from about 200 nsec to about 3 µsec.

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