True "Figure of Merit" for Power Electronics Switching Device

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Nearly three decades ago, specific on-state resistance (R_{sp}) and gate charge (Q_g) were introduced as the "Figure of Merits (FOM's)" to evaluate the potential of a given semiconductor technology for power electronics switching applications [1]. Since then, both of these FOM's have served as "industry standards" and have been extensively used by silicon power semiconductor industry to optimize the manufacturing technology [2, 3]. More than two decades ago, a new FOM [4, 5] that takes into account both electrical (σ) and thermal (λ) conductivities in addition to critical electric field strength (E_C) for avalanche breakdown was introduced in order to take advantage of unique material properties of Wide Bandgap (WBG) power semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN). Since then, several authors have proposed a number of FOM's. This paper will discuss all FOM's relevant to power semiconductor switching and converge on a "true" FOM that can be used to optimize power semiconductor technologies for performance and reliability [6, 7].

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[2] K. Shenai, "Optimally Scaled Low-Voltage Vertical Power DMOSFETs for High-Frequency Power Switching Applications," IEEE Trans. Electron Devices, vol. 37, no. 4, pp. 1141-1153, April 1990.

[3] K. Shenai, "Optimized Trench MOSFET Technologies for Power Devices," IEEE Trans. Electron Devices, vol. 39, no. 6, pp. 1435-1443, June 1992.

[4] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum Semiconductors for High-Power Electronics," IEEE Trans. Electron Devices, vol. 36, no. 9, pp. 1811-1823, September 1989.

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[6] K. Shenai, "Made-to-order Power Electronics," IEEE Spectrum, vol. 37, No. 7, pp. 50-55, July 2000 (**invited paper**).

[7] K. Shenai, "Switching megaWatts with Power Transistors," to appear in The Electrochemical Society Interface Magazine, vol. 22, no. 1, pp. 47-54, Spring 2013 (**invited paper**).