Quantum Tunneling for Ultra-Low-Power Scaled CMOS

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The dawn of tunnel diodes, commonly attributed to Leo Esaki in the late 1950's, predates much of the innovation and infrastructure investment into CMOS technology. But, the lack of a mass production process and inability to monolithically integrate these devices into complex circuits paved the way for the CMOS juggernaut seen today.

However, the unique negative differential resistance (NDR) systemic to all tunnel diodes provides a pathway to exploit new hybrid-CMOS circuit topologies with compact latches and reduced power consumption that could mitigate some of the bottlenecks perceived for scaled CMOS. A new paradigm of computing is possible, capitalizing upon transistor/tunnel diode integration if a viable Si-based tunnel diode could be developed. This talk will explore these opportunities.

Si-based resonant tunnel diodes (RTD) function via intraband tunneling through a confined quantum well state formed by double heterobarrier cladding. However, finding a suitable well and barrier material that are epitaxially compatible is a heated materials science topic. Si and SiGe provide a large valence band offset, but due to the large effective mass of holes, the valence band state becomes too diffuse to permit significant room temperature NDR behavior. Si/SiGe can provide a modest conduction band offset if a virtual SiGe substrate is used for strain engineering. Other barrier layers, including various oxides, are actively being pursued as a replacement, but these present a materials science compatibility problem that requires greater study.

By trading one materials science dilemma with another, studies of Si-based interband tunnel diodes were re-visited in Esaki-era alloy process. The key hindrance to this approach is dopant diffusion and segregation that prevents degenerate doping across a narrow p-n junction. This team pursued the usage of δ-doping and low temperature molecular beam epitaxy (LT-MBE) to suppress the dopant redistribution. If the growth and processing conditions are optimized, the δ-doping layers can create quantum wells leading to a Si-based resonant interband tunneling diode (RITD) configuration.

This talk will provide a background on Si-based tunnel diode devices and circuits and summarize the results of Si-based RITD device optimization, their monolithic integration with Si-based transistors and present a range of circuit prototyping. Recent developments to technology transfer this technology from molecular beam epitaxy (MBE) to standard CMOS chemical vapor deposition (CVD) will be highlighted. The extension of NDR to ultra-low voltage memory will also be discussed.