FDSOI technology: a power efficient solution down to 10nm

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1. Introduction

The Fully Depleted Silicon On Insulator (FDSOI) technology presents major advantages over the standard bulk CMOS one: an improved electrostatic control (that is considered today as a performance booster as much as channel strain [1]) and a high immunity to local variations (mismatch) thanks to its undoped channel [2]. A full 28nm platform functionality has been highlighted at the VLSI conference 2012 [3]. This paper first describes the technology with the associated electrical results (device and circuit level) and then provides solutions and trends for 14 and 10nm.

2. FDSOI technology

The FDSOI architecture is described in Figure 1 with a TEM picture of the nominal device. Tsi and BOX are 8nm and 25nm respectively. The channel is left undoped, leading to outstanding matching performance. An hybrid process scheme is used, by removing silicon film and BOX for back bias and for ESD devices. A highK/Metal gate stack is used and the threshold voltage (V_T) is adjusted by placing the right NWELL/GPN or PWELL/GPP doping below the devices. Raised Source/Drain processes are used to reduce the access resistances and then enable very good drivability. With such integration scheme, a complete platform has been built at 28nm with a complete set of devices [3].

3. Device and circuit electrical results

Logic devices exhibit very good static performance for N and PMOS (Fig. 2). These performances are very competitive compared to published Bulk and FinFET data. Excellent electrostatic control has already been reported, meaning that this technology is among the best candidates for technological nodes below 28nm. Excellent matching performances have been measured (twice better than doped devices), leading to improved stability at the SRAM level. Thanks to FDSOI technology, a clear improvement of the speed power tradeoff has been measured on wafers: up to 30% speed improvement at nominal VDD and up to 400% speed gain is achieved at very low supply voltage (Fig.3). For a given speed, the FDSOI circuit supply voltage can be reduced by 150mV, leading to 50% gain in Power consumption. Multi core A9 circuit have been processed and frequency of 800MHz have been demonstrated at VDD=0.6V. These results highlight the fact that FDSOI technology is the most powerful technology in terms of power efficiency.

4. Scaling down to 10nm

The scaling of both silicon film and BOX is mandatory to control further short channel effects down to 10nm node. With such physical dimensions (Fig.4), the electrostatic control will be ensured. Regarding the performance improvement, strain SOI substrates can bring 20% performance gain for NMOS. For the PMOS, a SiGe channel is introduced for current improvement and V_T adjustment. In order to achieve ultra-low access resistance in-situ doped S/D are raised by selective epitaxy. The raised SiC-P and SiGe-B S/D (for NMOS and PMOS respectively), are used as strain boosters of performance. With such boosters, ITRS criteria will be fulfilled down to 10nm.

5. Conclusion

This paper gives an overview of the last results obtained with the FDSOI technology. Clear demonstration of its power efficiency has been done and its scalability down to 10nm node has been shown.

Acknowledgements

Special thanks to our ST and IBM colleagues (especially Franck Arnaud and Michel Haond). This work has been pursued in the frame of the ST/IBM/LETI collaboration, with support of Reaching22 and Dynamic ULP projects. The ANR (French National Research Agency) is grandly acknowledged for its support in these developments in the frame of the Equipex FDSOI11 project.

References

[1] C. Fenouillet-Beranger et al, IEDM 2007, pp. 267-270 ; [2] K. Cheng et al, IEDM 2009, pp. 321-324 [3] J. Hartmann et al, http://www.soiconsortium.org/fully-depleted-soi/presentations/december-2012/;

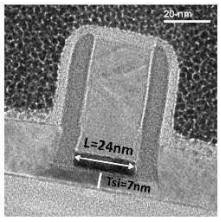

Fig. 1 : TEM picture of a FDSOI device

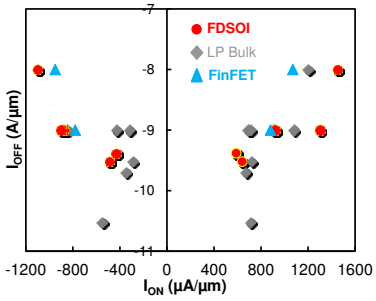

Fig. 2: Benchmarking of $I_{ON}(I_{OFF})$ tradeoff for NMOS and PMOS devices

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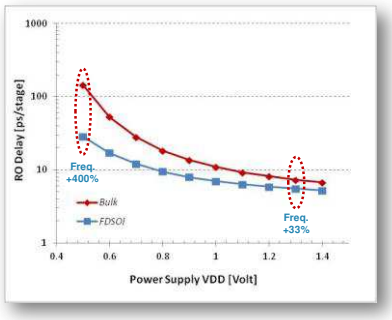

Fig. 3: RO delay evolution vs Vdd for Bulk and FDSOI technologies

Node	28nm	14nm	10nm
T_{SOI} (nm)	7.5	6.5	6
T_{BOX} (nm)	25	20	15

Fig. 4: Scaling rules of FDSOI devices down to 8nm node.