High Voltage GaN Technology in a Silicon CMOS Environment: Challenges and Opportunities

H. Rusty Harris[a], Derek W. Johnson[a], Richard J. W. Hill[b], Edwin L. Piner[c], Man Hoi Wong[b], Rinus T. P. Lee[b]

a) Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843-3128

b) SEMATECH, 257 Fuller Road, Albany, NY.

c) Department of Physics, Texas State University, San Marcos, TX 78666

Texas A&M

The escalating needs of the energy industry dictate the implementation of higher voltage integrated and discreet technology in a high volume manufacturing environment. The silicon CMOS industry has years of high volume manufacturing, but the distinct material needs of high voltage device technology conflicts with the pristine clean materials environment of Si CMOS. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the two leading material sets in high voltage device research and product lines, but lateral GaN devices lend themselves to more immediate, natural integration into Si CMOS. In this paper, we explore the challenges of contamination and tool protocol, development of Au-free contacts that are compatible with CMOS equipment, understanding of alternate wafer challenges, and dielectric issues with respect to device operation.