"How Far Can We Push Si CMOS and What are the Alternatives for Future Nanoelectronics?"

Abstract
Si CMOS technology has dominated the microelectronics industry, with continued scaling. However, future scaling is reaching practical and fundamental limits. Currently, strained-Si channel with high-k/metal gate is the dominant technology. Si FinFETs have provided further innovation to improve electrostatic control of the channel and thus reduce leakage. However, performance enhancement of Si CMOS is beginning to saturate with scaling to nanoscale. To go beyond these limits novel materials and structures are being aggressively studied. Higher mobility semiconductors, like Ge, GeSn and III-Vs, together with innovative device structures could increase drive current and reduce power consumption and delay. These materials have also opened totally new areas of applications, e.g., photonics. Carbon nanotubes and graphene offer very high mobility, excellent electrostatic control of the channel but have problems in manufacturability. Graphene also has the problem of ~0 bandgap making it not very useful for logic. Recently 2D materials like metal sulfides, tellurides and selenides have emerged as potential candidates for nanoscale devices.

Is Ge PMOS and III-V NMOS co-integration on Si feasible or a headache for the manufacturing folks? Can we have all Ge or all III-V CMOS or it is just a fantasy? Can CNT FETs become manufacturable? Are 2D materials more promising? This panel will try to answer some of these questions.

Moderator
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